

# UM3/UM6 SYSTEM BLOCK DIAGRAM

## POWER

**AC/BATT CONNECTOR**  
PG 53

**SYSTEM RESET CIRCUIT** PG 42

**BATT CHARGER** PG 45

**RUN POWER SW**  
+3.3V\_SUS/+5V\_SUS  
+5V/+3.3V/+1.8V PG 52

**CPU VR** PG 51

**DC/DC**  
+3.3V\_ALW/+5V\_ALW/  
+15V\_ALW PG 46

**REGULATOR**  
+1.5V\_SUS/+0.75V\_DDR\_VTT PG 47  
+1.05V\_PCH PG 48  
+1.05V\_VTT PG 49

**THERMAL**  
SMSC1422 PG 38

**CLOCK**  
SLG8SP585VTR  
(QFN-32) PG 15

**DDR3-SODIMM1**  
RVS Type PG 13

**DDR3-SODIMM2**  
RVS Type PG 14

Dual Channel DDR3  
800/1066 1.5V

**Arrandale**  
( rPGA 989 )  
PG 3,4,5,6

**ATI M92-LP S2**  
**PCI EXPRESS GFX**  
631 uFCBGA 23mm\*23mm  
PG 16,17,18,19,20,21,22

**DDR3 x 4**  
(512M 64bits)  
PG 22

**Panel Connector** PG 24  
**HDMI CONN.** PG 24  
**CRT CONN.** PG 25

**SATA-ODD** PG 35

**SATA-HDD** PG 35

**USB conn x 1** PG 33

**Bluetooth BTB Conn**  
BT365 PG 32

**Camera** PG 24  
To LCD Conn

**AUDIO/AMP**  
ALC269Q-GR PG 39

**A- MIC conn** PG 39

**Audio SPK conn** PG 39

**Audio Jacks x2** PG 26

**USER INTERFACE** PG 37

**PCH**  
(HM55)  
PG 7,8,9,10,11,12

**KBC**  
ITE8502 PG 29

**FLASH**  
4Mbytes PG 30

**Keyboard** PG 36

**FLASH**  
1Mbytes PG 30

**Touchpad** PG 36

**LOM**  
RTL8103E PG 41  
**MINI-CARD**  
WLAN PG 32  
**MINI-CARD**  
WWAN PG 31

**USB conn x 2**  
**CARD READER**  
RTS5159

**IO Board** PG 26


**VER :C3B**  
**PWA:**  
**PWB:**

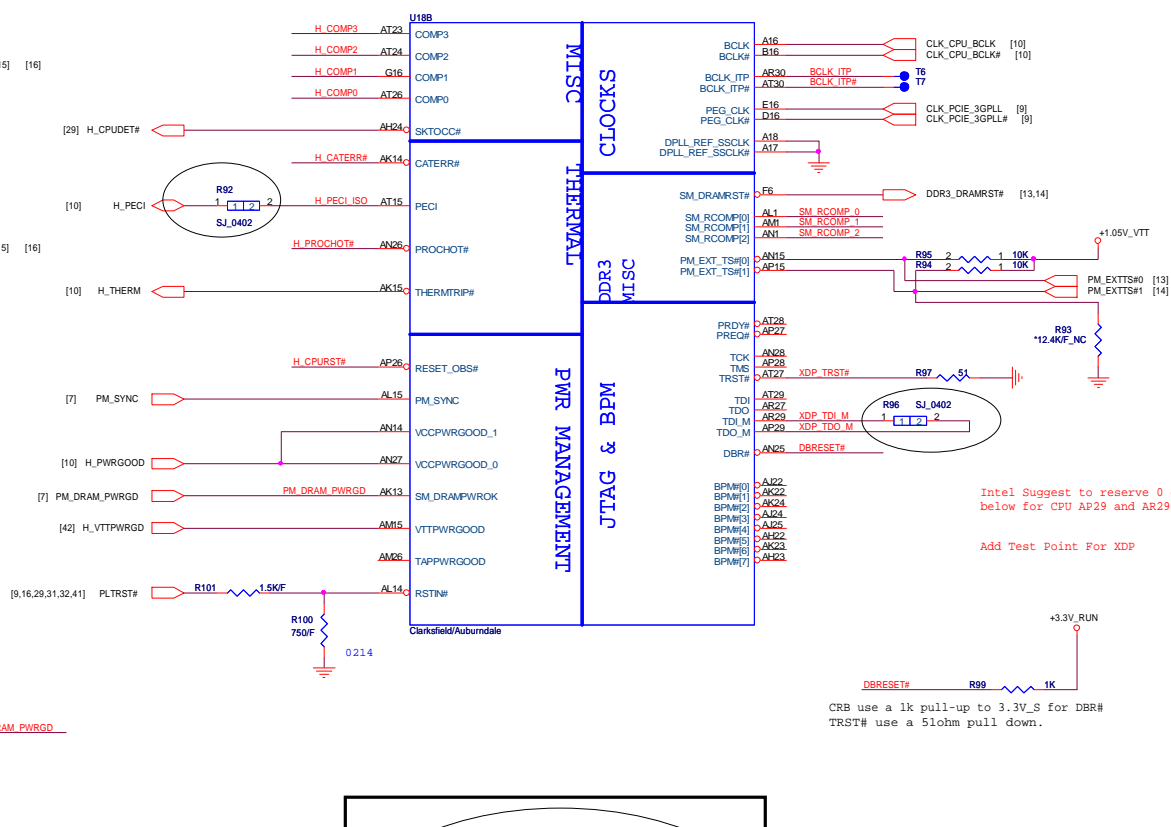
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25	CRT CONN
26	DB CONN / R5U230
27	BLANK PAGE
28	BLANK PAGE
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34	BLANK PAGE
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49	1.05_VTT(TPS51218)
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Power States

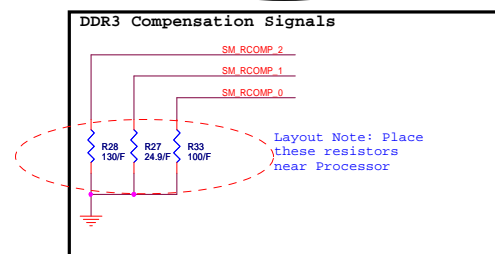
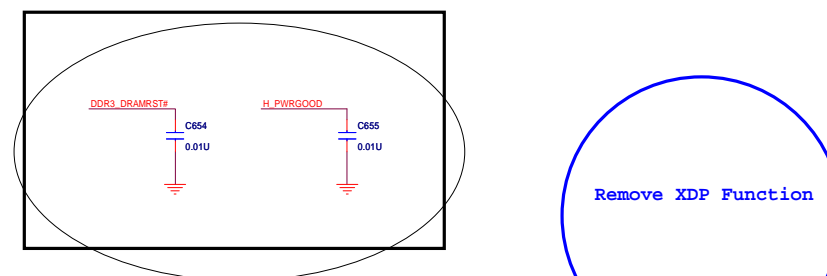
POWER PLANE	VOLTAGE	PAGE	DESCRIPTION	CONTROL SIGNAL	ACTIVE IN
+PWR_SRC	10V~+19V	24,45,46,47,48,49,50,51	MAIN POWER		S0~S5
+RTC_CELL	+3.0V~+3.3V	08,11,29,30	RTC		S0~S5
+5V_ALW	+5V	37,44,46,47,49,50,53	LARGE POWER	ALW_ON	S0~S5
+3.3V_ALW	+3.3V	29,30,37,44,45,46,51,52,53	8051 POWER	3.3V_ALW_ON	S0~S5
+5V_SUS	+5V	11,26,33,37,46,48,51,52	SLP_S5# CTRLD POWER	SUS_ON	
+3.3V_SUS	+3.3V	07,08,09,10,11,,24,36,37,41,42,44,47,50,52	SLP_S5# CTRLD POWER	SUS_ON	
+1.5V_SUS	+1.5V	03,05,13,14,47,50,52	SODIMM POWER	SUS_ON	
+0.75V_DDR_VTT	+0.75V	13,14,47	SODIMM POWER	RUN_ON	
+5V_RUN	+5V	11,18,24,25,35,36,37,38,39,51,52	SLP_S3# CTRLD POWER	RUN_ON	
+3.3V_RUN	+3.3V	3,7,8,9,10,11,13,14,15,17,19,24,25,26,29,30,31,32,35,38,39,41,42,51,52	SLP_S3# CTRLD POWER	RUN_ON	
+1.8V_RUN	+1.8V	05,11,44	SDVO POWER	RUN_ON	
+1.5V_RUN	+1.5V	11,18,19,20,31,32,52	VGA POWER	RUN_ON	
+VCC_GFX_CORE	+0.9V~+1.2V	18,21,50	VGA POWER	GFX_ON	
+1.1V_GFX_PCIE	+1.1V	18,50	VGA POWER	GFX_+1.1_EN	
+1.8V_RUN_GFX	+1.8V	17,18,21,22,44	VGA POWER	GFX_+1.8_EN	
+1.05V_PCH	+1.05V	07,08,09,11,15,48	PCH POWER	RUN_ON	
+VCC_CORE	+0.7V~+1.77V	05,51	CPU CORE POWER	IMVP_VR_ON	
+LCDVCC	+3.3V	24	LCD Power	LCDVCC_TST_EN & ENVDD	
+1.05V_VTT	+1.1V	03,05,10,11,49	CPU POWER	RUN_ON	

GND PLANE	PAGE	DESCRIPTION
 GND	ALL	

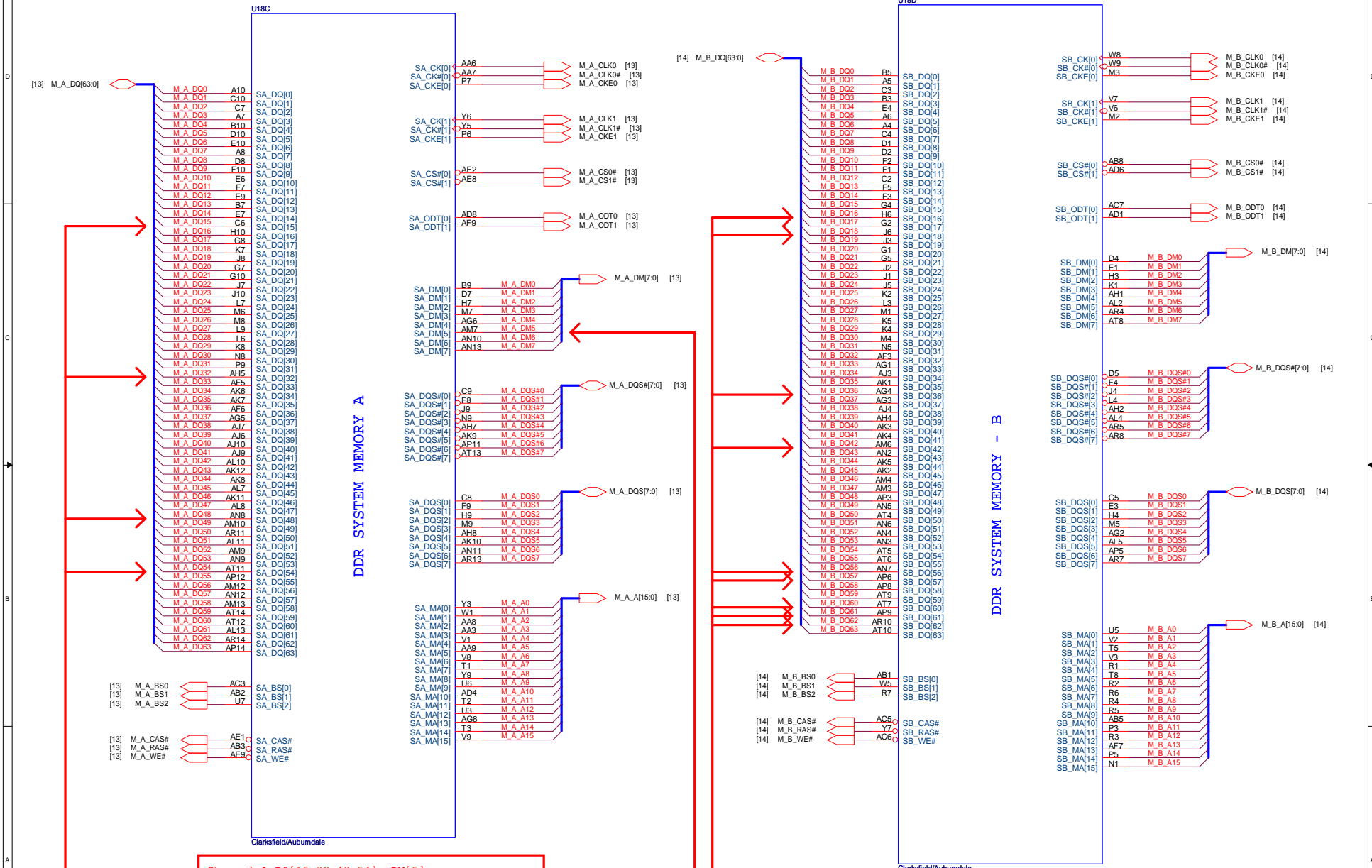


### Add Test Point For XDP

CRB use a 1k pull-up to 3.3V\_S for DBR#  
TRST# use a 51ohm pull down.



AUBURNDALE/CLARKSFIELD PROCESSOR (DDR3)

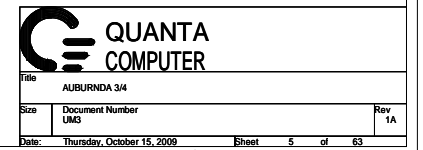


Channel A DQ[15,32,48,54], DM[5]  
Requires minimum 12mils spacing  
with all other signals, including data signals.

Channel B DQ[16,18,36,42,56,57,60,61,62]  
Requires minimum 12mils spacing  
with all other signals, including data signals.

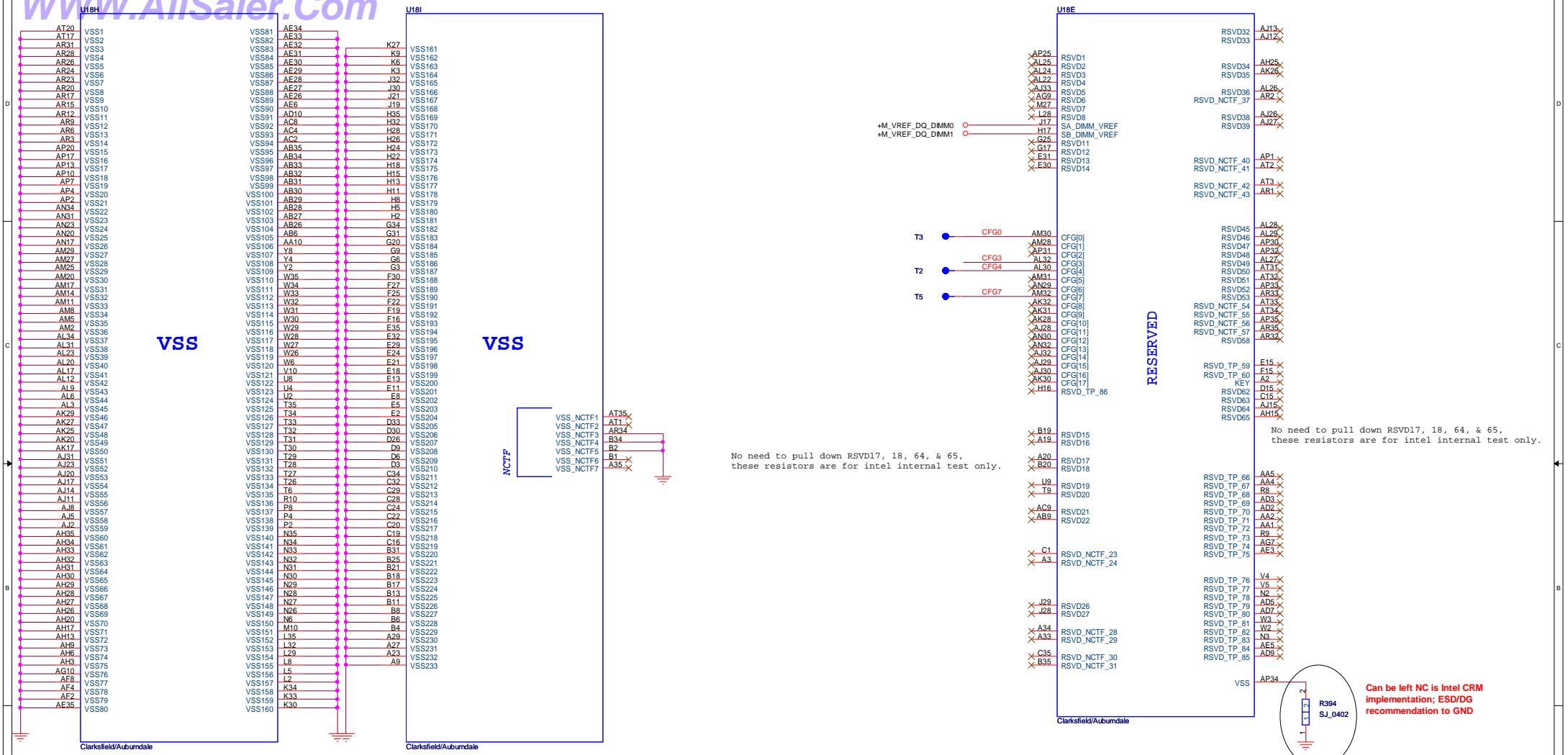
**QUANTA  
COMPUTER**

Title AUBURND 2/4		
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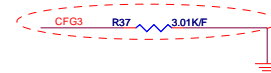


# AUBURNDALE/CLARKSFIELD PROCESSOR (GND)

# AUBURNDALE/CLARKSFIELD PROCESSOR ( RESERVED, CFG)



The Clarkfield processor's PCI Express interface may not meet PCI Express 2.0 jitter specifications. Intel recommends placing a 3.01K +/- 5% pull down resistor to VSS on CFG[7] pin for both rPGA and BGA components. This pull down resistor should be removed when this issue is fixed.



	1	0
CFG4 (Display Port Presence)	Disabled; No Physical Display Port attached to Embedded Display Port	Enabled; An external Display port device is connected to the Embedded Display port
CFG0 (PCI-Epress Configuration Select)	Single PEG	Bifurcation enabled
CFG3 (PCI-Epress Static Lane Reversal)	Normal Operation	Lane Numbers Reversed

**QUANTA COMPUTER**

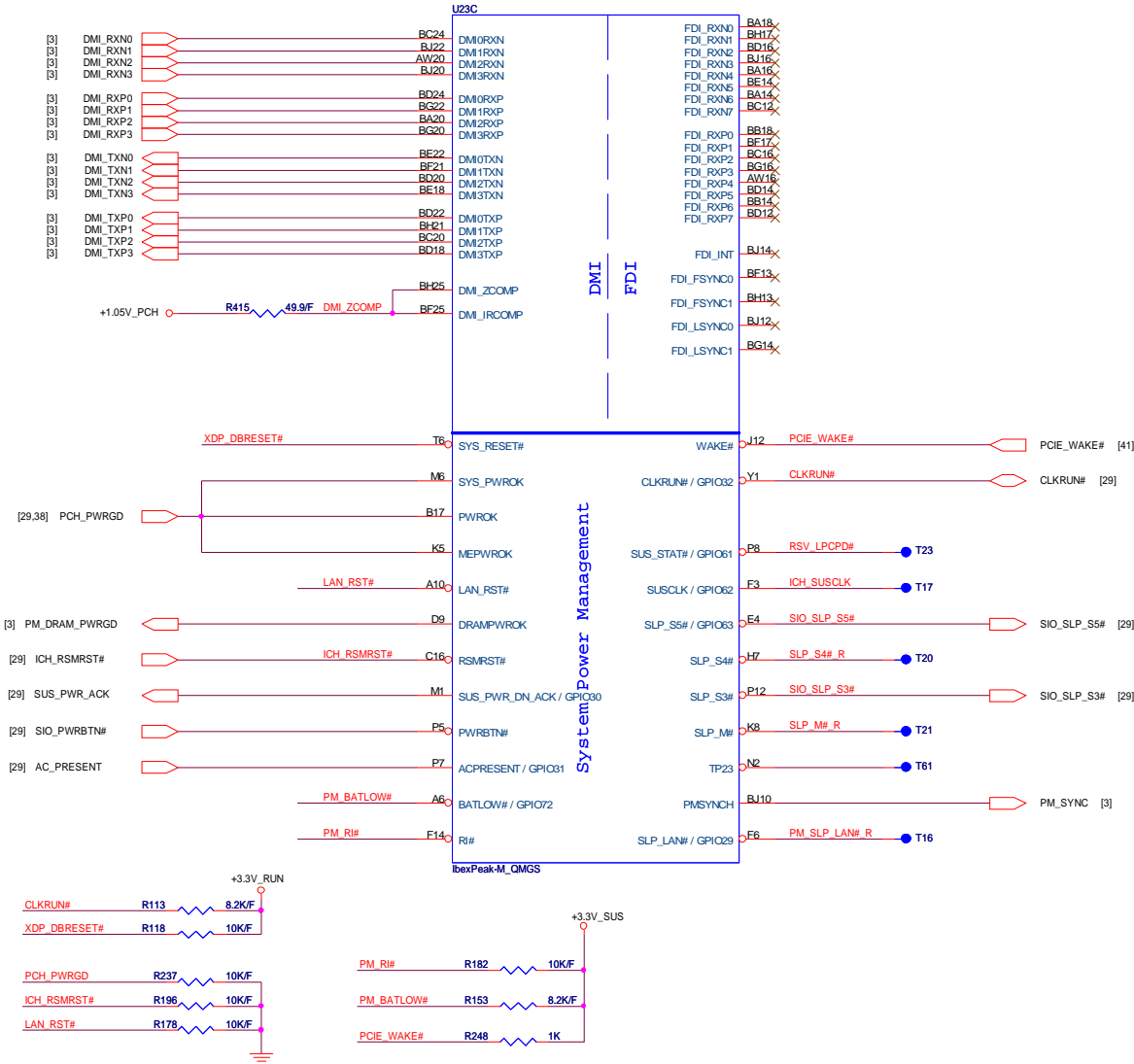
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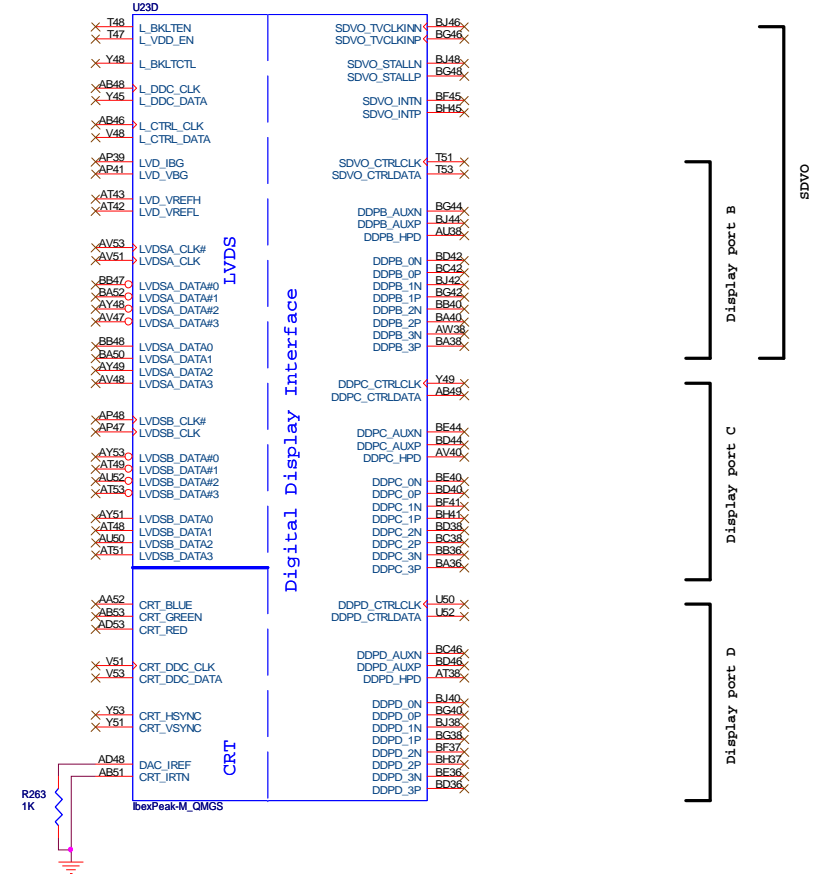
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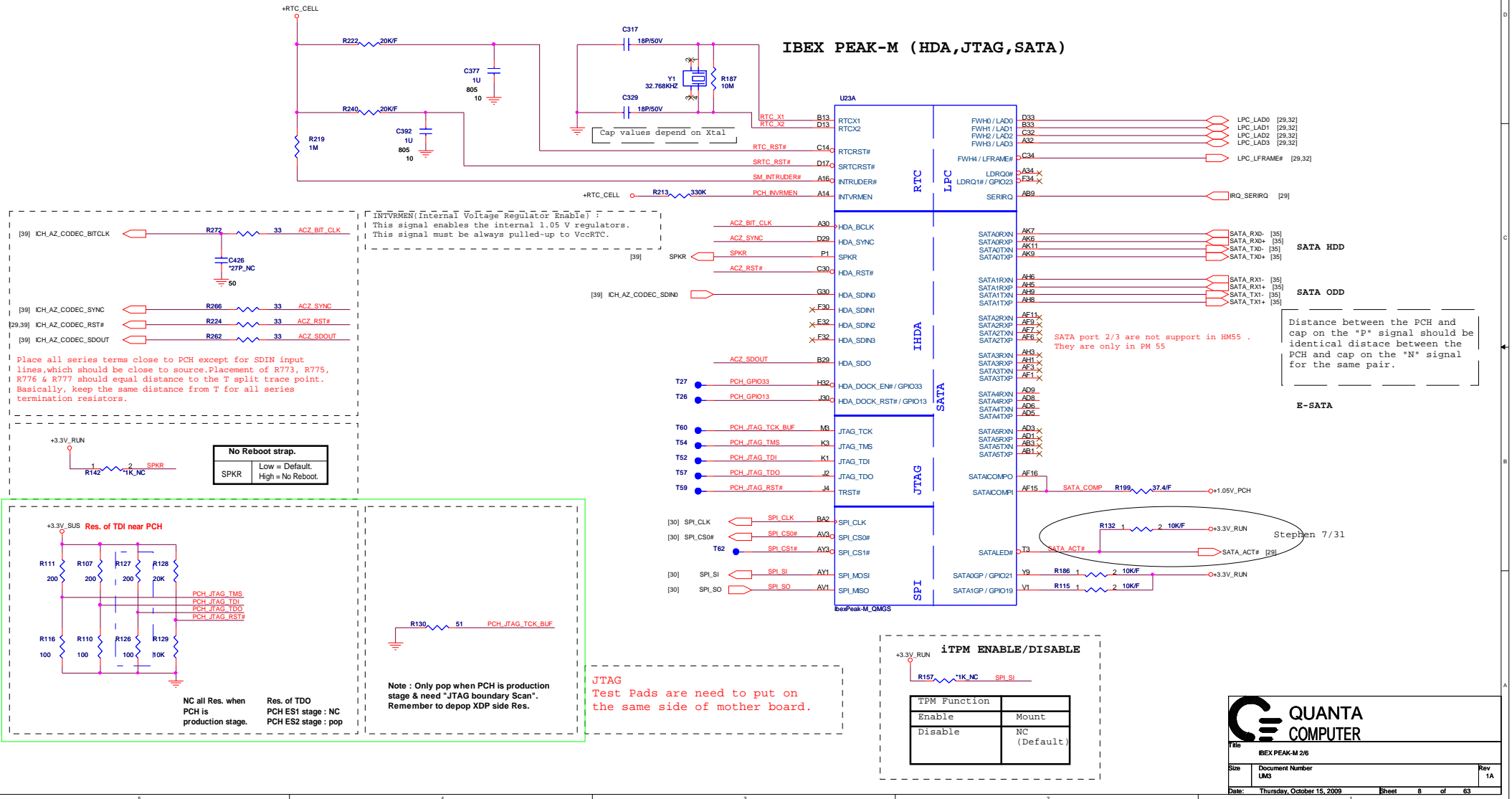


IBEX PEAK-M (LVDS, DDI)



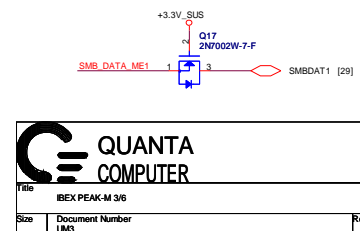
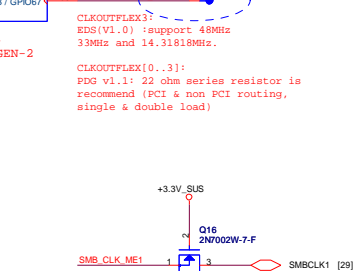
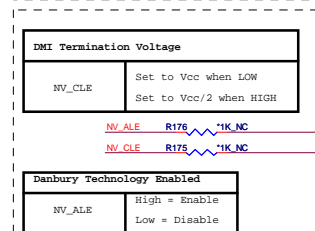
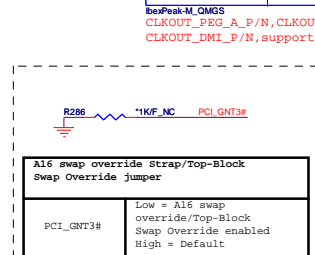
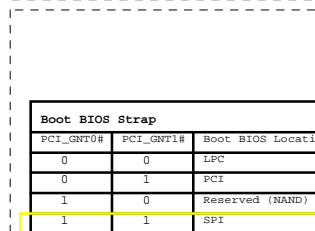
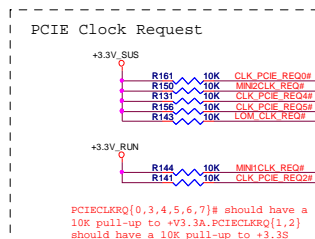
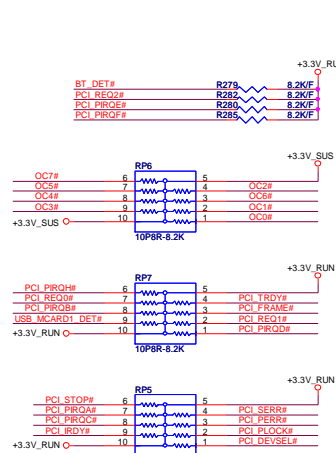
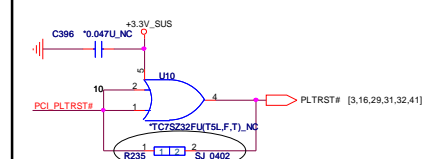
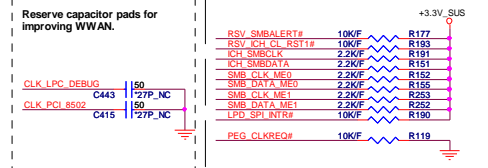
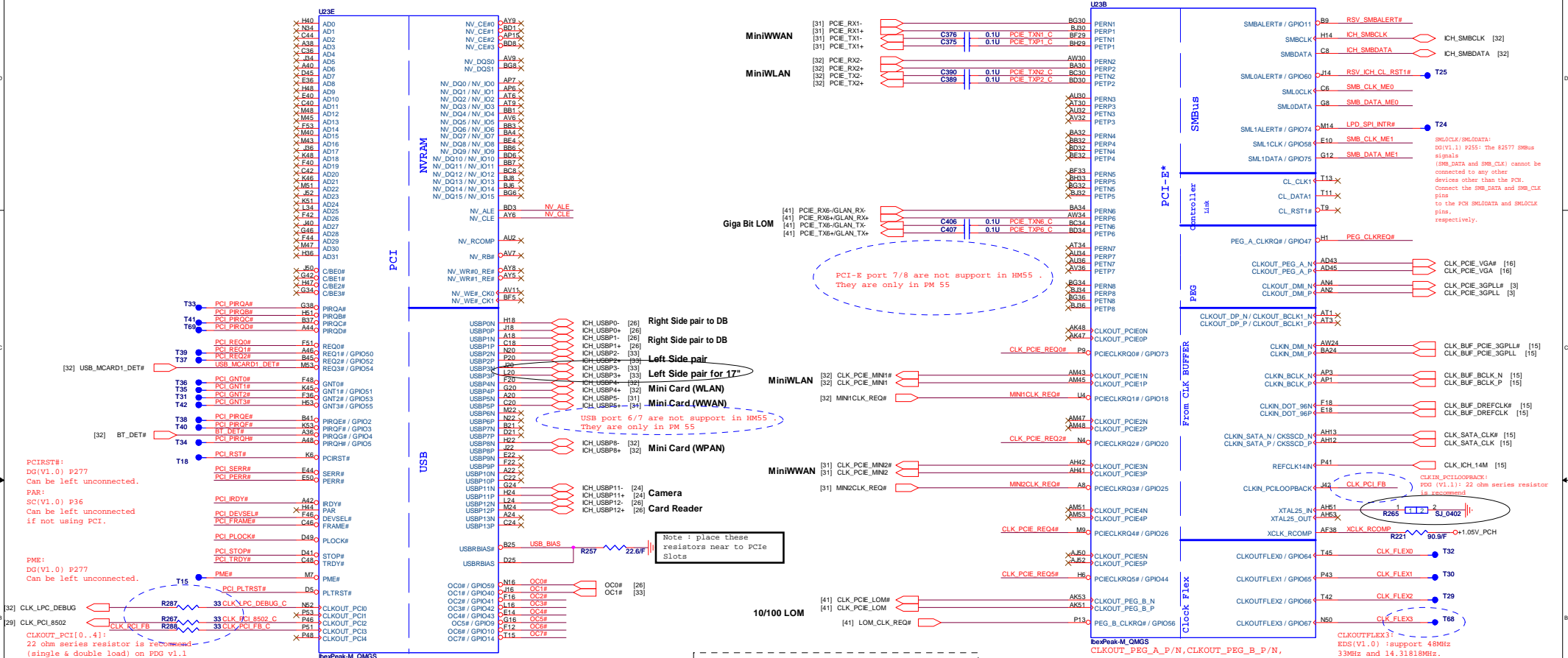


# IBEX PEAK-M (HDA,JTAG,SATA)

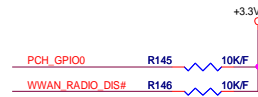
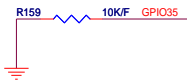
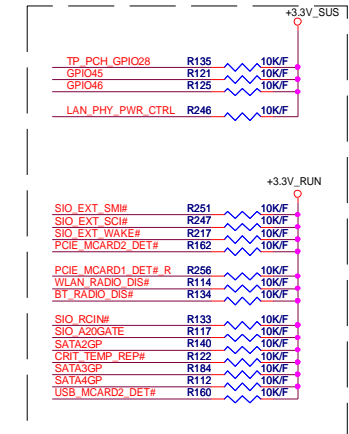
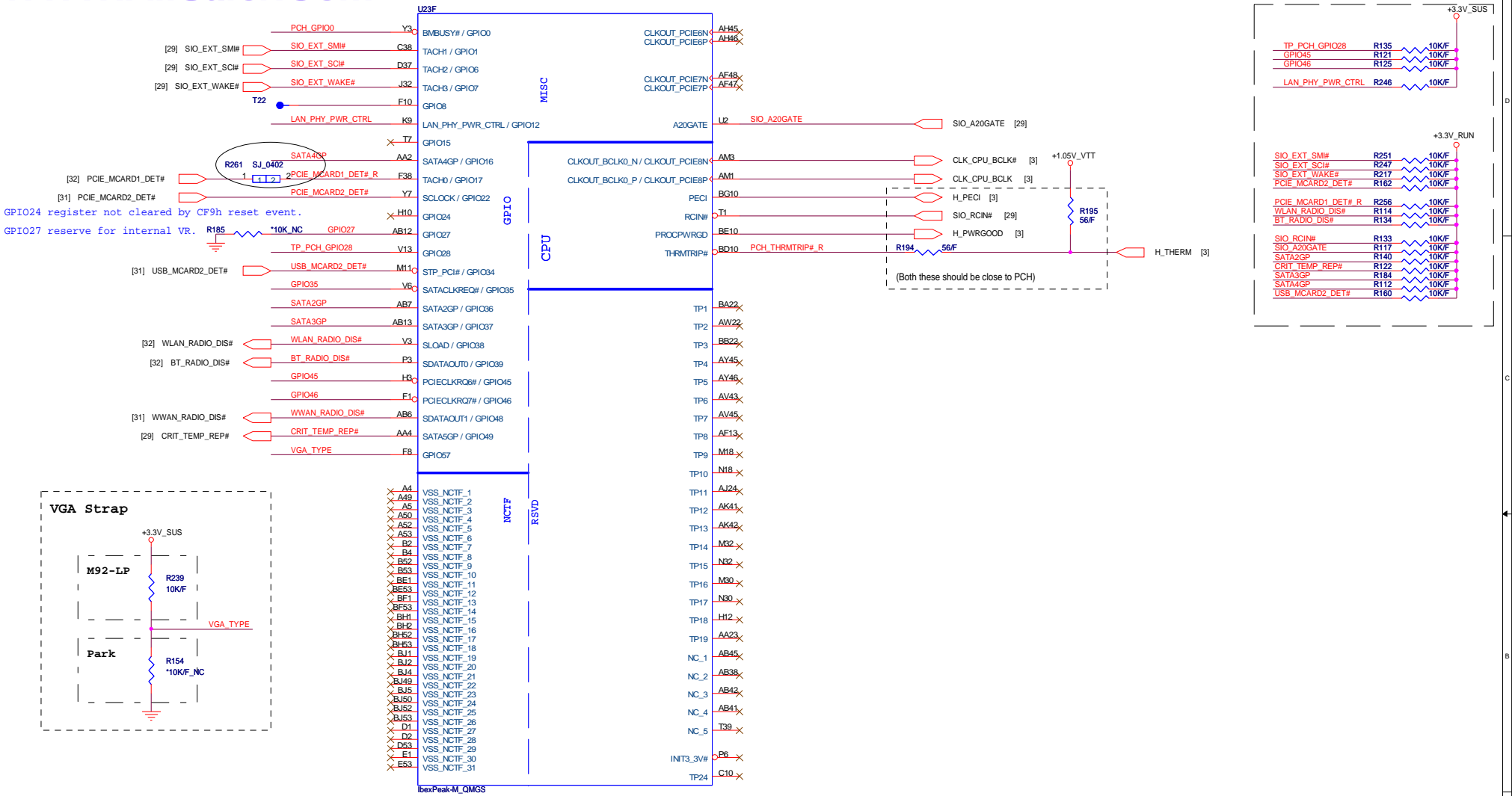




Place TX DC blocking caps close PCH.



# IBEX PEAK-M (GPIO,VSS\_NCTF,RSVD)



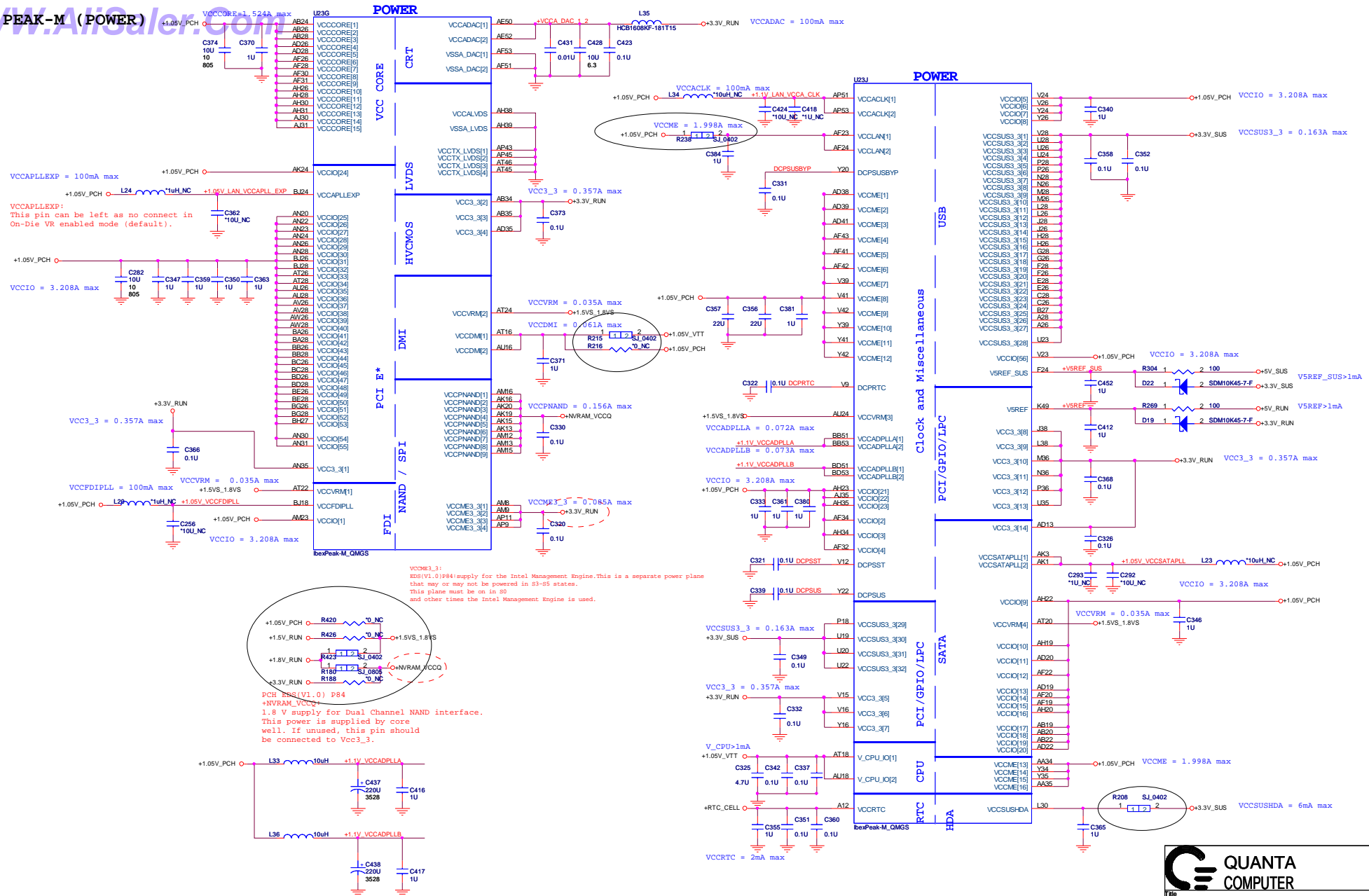
BMBUSY#:(Intel feedback)  
Follow CRB checklist, 1K is for intel BIOS validation purpose.

BMBUSY#:  
If not used, require a weak pull-up (8.2- 10K to 10 kΩ) to Vcc3.3.  
CRB(V1.0)P28: it has 1K PU and 100 ohm on this net for validation purpose.

WWAN\_RADIO\_DIS# 1-X High = Strong (Default)



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IBEX PEAK-M (GND)

U23H		
AB16	VSS[0]	
AA19	VSS[1]	VSS[80] AK30
AA20	VSS[2]	VSS[81] AK31
AA22	VSS[3]	VSS[82] AK32
AA23	VSS[4]	VSS[83] AK33
AA24	VSS[5]	VSS[84] AK34
AA26	VSS[6]	VSS[85] AK35
AA28	VSS[7]	VSS[86] AK36
AA30	VSS[8]	VSS[87] AK37
AA31	VSS[9]	VSS[88] AK38
AA32	VSS[10]	VSS[89] AK39
AB11	VSS[11]	VSS[90] AK40
AB15	VSS[12]	VSS[91] AK41
AB23	VSS[13]	VSS[92] AK42
AB30	VSS[14]	VSS[93] AK43
AB31	VSS[15]	VSS[94] AK44
AB32	VSS[16]	VSS[95] AK45
AB33	VSS[17]	VSS[96] AK46
AB34	VSS[18]	VSS[97] AK47
AB37	VSS[19]	VSS[98] AK48
AB5	VSS[20]	VSS[99] AK49
AB8	VSS[21]	VSS[100] AK50
AC2	VSS[22]	VSS[101] AK51
AC52	VSS[23]	VSS[102] AK52
AD11	VSS[24]	VSS[103] AK53
AD12	VSS[25]	VSS[104] AK54
AD16	VSS[26]	VSS[105] AK55
AD2	VSS[27]	VSS[106] AK56
AD30	VSS[28]	VSS[107] AK57
AD31	VSS[29]	VSS[108] AK58
AD32	VSS[30]	VSS[109] AK59
AD34	VSS[31]	VSS[110] AK60
AU22	VSS[32]	VSS[111] AK61
AD42	VSS[33]	VSS[112] AK62
AD46	VSS[34]	VSS[113] AK63
AD49	VSS[35]	VSS[114] AK64
AD7	VSS[36]	VSS[115] AK65
AE2	VSS[37]	VSS[116] AK66
AE4	VSS[38]	VSS[117] AK67
AF12	VSS[39]	VSS[118] AK68
Y13	VSS[40]	VSS[119] AK69
AH49	VSS[41]	VSS[120] AK70
AU4	VSS[42]	VSS[121] AK71
AF36	VSS[43]	VSS[122] AK72
AP13	VSS[44]	VSS[123] AK73
AN4	VSS[45]	VSS[124] AK74
AF45	VSS[46]	VSS[125] AK75
AF46	VSS[47]	VSS[126] AK76
AF49	VSS[48]	VSS[127] AK77
AF5	VSS[49]	VSS[128] AK78
AF8	VSS[50]	VSS[129] AK79
AG2	VSS[51]	VSS[130] AK80
AG52	VSS[52]	VSS[131] AK81
AH11	VSS[53]	VSS[132] AK82
AH16	VSS[54]	VSS[133] AK83
AH16	VSS[55]	VSS[134] AK84
AH24	VSS[56]	VSS[135] AK85
AH32	VSS[57]	VSS[136] AK86
AV18	VSS[58]	VSS[137] AK87
AH43	VSS[59]	VSS[138] AK88
AH47	VSS[60]	VSS[139] AK89
AH7	VSS[61]	VSS[140] AK90
AJ19	VSS[62]	VSS[141] AK91
AJ2	VSS[63]	VSS[142] AK92
AJ20	VSS[64]	VSS[143] AK93
AD2	VSS[65]	VSS[144] AK94
AD3	VSS[66]	VSS[145] AK95
AJ6	VSS[67]	VSS[146] AK96
AJ28	VSS[68]	VSS[147] AK97
AJ32	VSS[69]	VSS[148] AK98
AJ4	VSS[70]	VSS[149] AK99
AT5	VSS[71]	VSS[150] AK100
AJ4	VSS[72]	VSS[151] AK101
AK12	VSS[73]	VSS[152] AK102
AM11	VSS[74]	VSS[153] AK103
AN19	VSS[75]	VSS[154] AK104
AK26	VSS[76]	VSS[155] AK105
AK27	VSS[77]	VSS[156] AK106
AK3	VSS[78]	VSS[157] AK107
AK28	VSS[79]	VSS[158] AK108

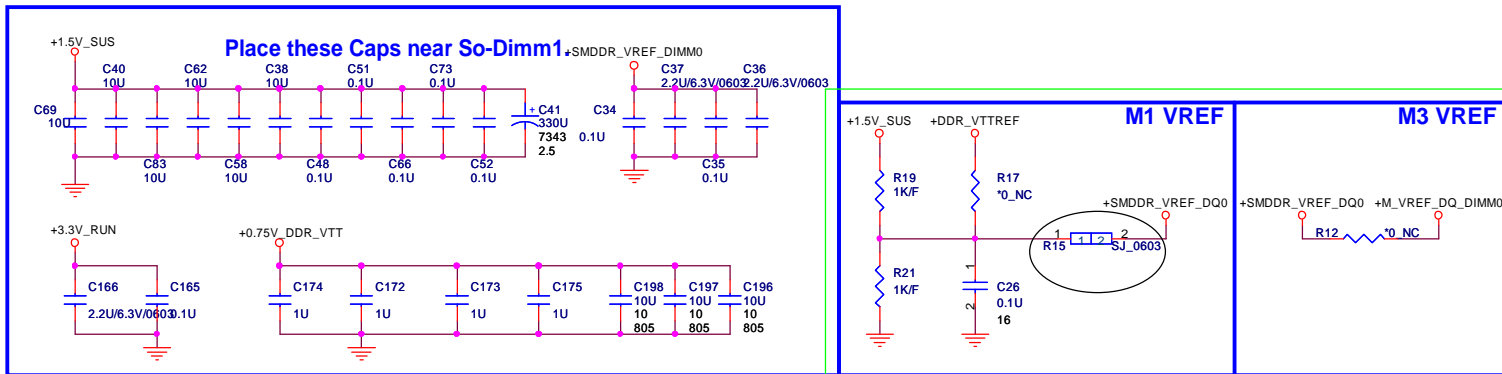
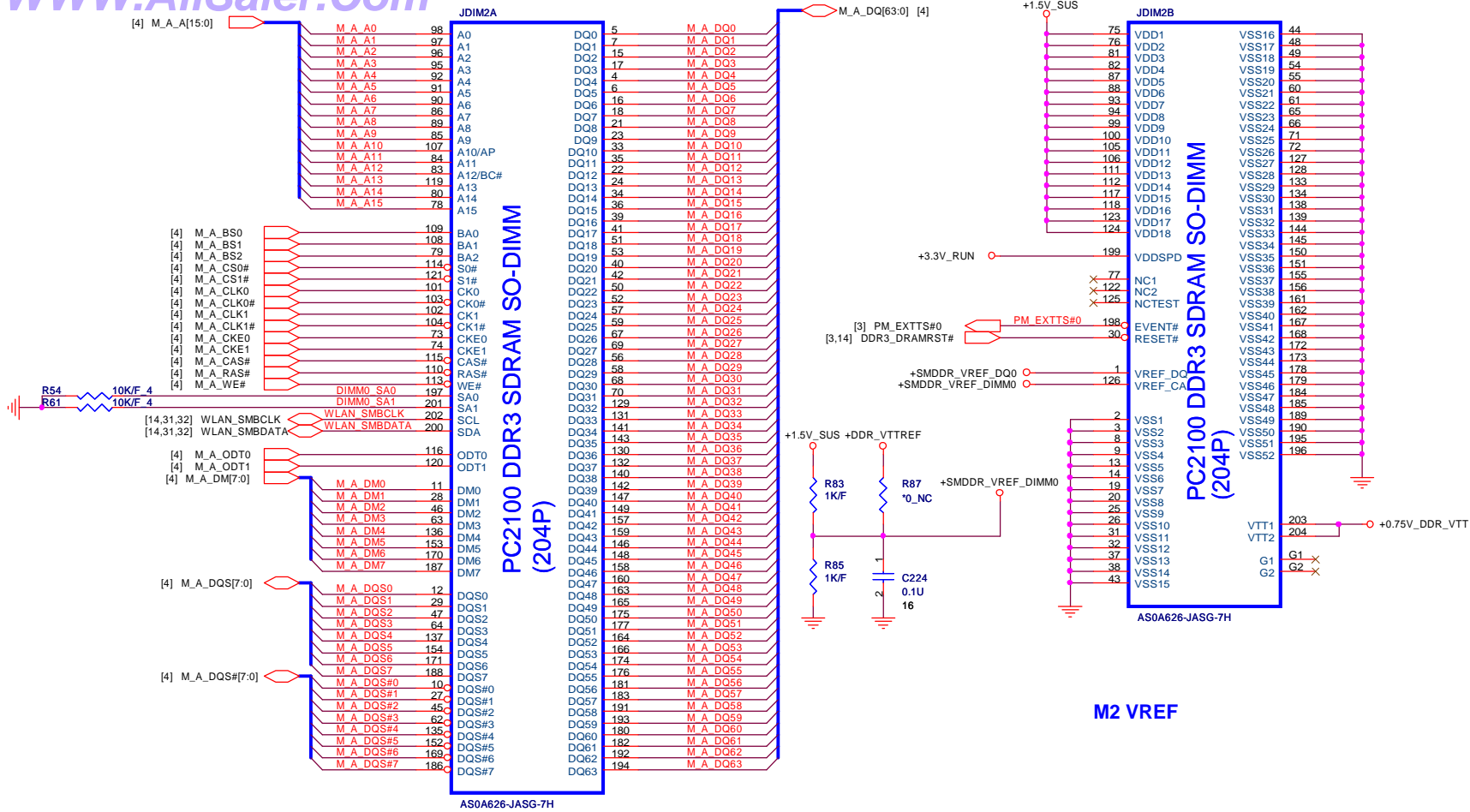
BoxPeak-M\_QMGS

U23I		
AJ7	VSS[159]	VSS[259] H49
B11	VSS[160]	VSS[260] H5
B15	VSS[161]	VSS[261] J24
B19	VSS[162]	VSS[262] K11
B21	VSS[163]	VSS[263] K43
B31	VSS[164]	VSS[264] K47
B35	VSS[165]	VSS[265] L14
B39	VSS[166]	VSS[266] L18
B43	VSS[167]	VSS[267] L2
B7	VSS[168]	VSS[268] L22
BB12	VSS[169]	VSS[269] L32
BB12	VSS[170]	VSS[270] L36
BB16	VSS[171]	VSS[271] L40
BB20	VSS[172]	VSS[272] M2
BB24	VSS[173]	VSS[273] M12
BB30	VSS[174]	VSS[274] M16
BB34	VSS[175]	VSS[275] M20
BB38	VSS[176]	VSS[276] M24
BB42	VSS[177]	VSS[277] M28
BB46	VSS[178]	VSS[278] M32
BB50	VSS[179]	VSS[279] M36
BB54	VSS[180]	VSS[280] M40
BB58	VSS[181]	VSS[281] M44
BC10	VSS[182]	VSS[282] M48
BC14	VSS[183]	VSS[283] M52
BC18	VSS[184]	VSS[284] M56
BC22	VSS[185]	VSS[285] M60
BC26	VSS[186]	VSS[286] M64
BC30	VSS[187]	VSS[287] M68
BC34	VSS[188]	VSS[288] M72
BC38	VSS[189]	VSS[289] M76
BC42	VSS[190]	VSS[290] M80
BC46	VSS[191]	VSS[291] M84
BC50	VSS[192]	VSS[292] M88
BC54	VSS[193]	VSS[293] M92
BC58	VSS[194]	VSS[294] M96
BE12	VSS[195]	VSS[295] R52
BE16	VSS[196]	VSS[296] R56
BE20	VSS[197]	VSS[297] R60
BE24	VSS[198]	VSS[298] R64
BE28	VSS[199]	VSS[299] R68
BE32	VSS[200]	VSS[300] R72
BE36	VSS[201]	VSS[301] R76
BE40	VSS[202]	VSS[302] R80
BE44	VSS[203]	VSS[303] R84
BE48	VSS[204]	VSS[304] R88
BE52	VSS[205]	VSS[305] R92
BE56	VSS[206]	VSS[306] R96
BE60	VSS[207]	VSS[307] R100
BE64	VSS[208]	VSS[308] R104
BE68	VSS[209]	VSS[309] R108
BE72	VSS[210]	VSS[310] R112
BE76	VSS[211]	VSS[311] R116
BE80	VSS[212]	VSS[312] R120
BE84	VSS[213]	VSS[313] R124
BE88	VSS[214]	VSS[314] R128
BE92	VSS[215]	VSS[315] R132
BE96	VSS[216]	VSS[316] R136
BE100	VSS[217]	VSS[317] R140
BE104	VSS[218]	VSS[318] R144
BE108	VSS[219]	VSS[319] R148
BE112	VSS[220]	VSS[320] R152
BE116	VSS[221]	VSS[321] R156
BE120	VSS[222]	VSS[322] R160
BE124	VSS[223]	VSS[323] R164
BE128	VSS[224]	VSS[324] R168
BE132	VSS[225]	VSS[325] R172
BE136	VSS[226]	VSS[326] R176
BE140	VSS[227]	VSS[327] R180
BE144	VSS[228]	VSS[328] R184
BE148	VSS[229]	VSS[329] R188
BE152	VSS[230]	VSS[330] R192
BE156	VSS[231]	VSS[331] R196
BE160	VSS[232]	VSS[332] R200
BE164	VSS[233]	VSS[333] R204
BE168	VSS[234]	VSS[334] R208
BE172	VSS[235]	VSS[335] R212
BE176	VSS[236]	VSS[336] R216
BE180	VSS[237]	VSS[337] R220
BE184	VSS[238]	VSS[338] R224
BE188	VSS[239]	VSS[339] R228
BE192	VSS[240]	VSS[340] R232
BE196	VSS[241]	VSS[341] R236
BE200	VSS[242]	VSS[342] R240
BE204	VSS[243]	VSS[343] R244
BE208	VSS[244]	VSS[344] R248
BE212	VSS[245]	VSS[345] R252
BE216	VSS[246]	VSS[346] R256
BE220	VSS[247]	VSS[347] R260
BE224	VSS[248]	VSS[348] R264
BE228	VSS[249]	VSS[349] R268
BE232	VSS[250]	VSS[350] R272
BE236	VSS[251]	VSS[351] R276
BE240	VSS[252]	VSS[352] R280
BE244	VSS[253]	VSS[353] R284
BE248	VSS[254]	VSS[354] R288
BE252	VSS[255]	VSS[355] R292
BE256	VSS[256]	VSS[356] R296
BE260	VSS[257]	VSS[357] R300
BE264	VSS[258]	VSS[358] R304

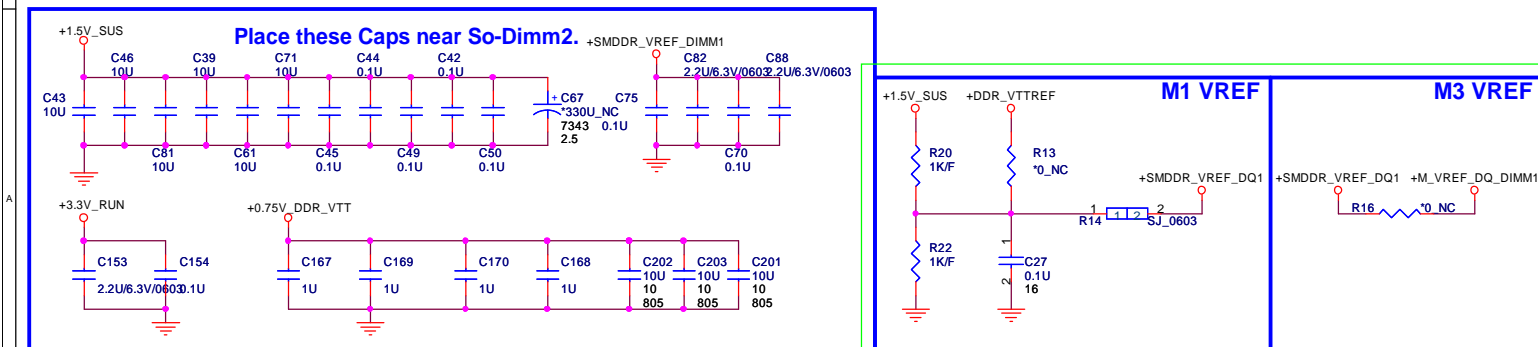
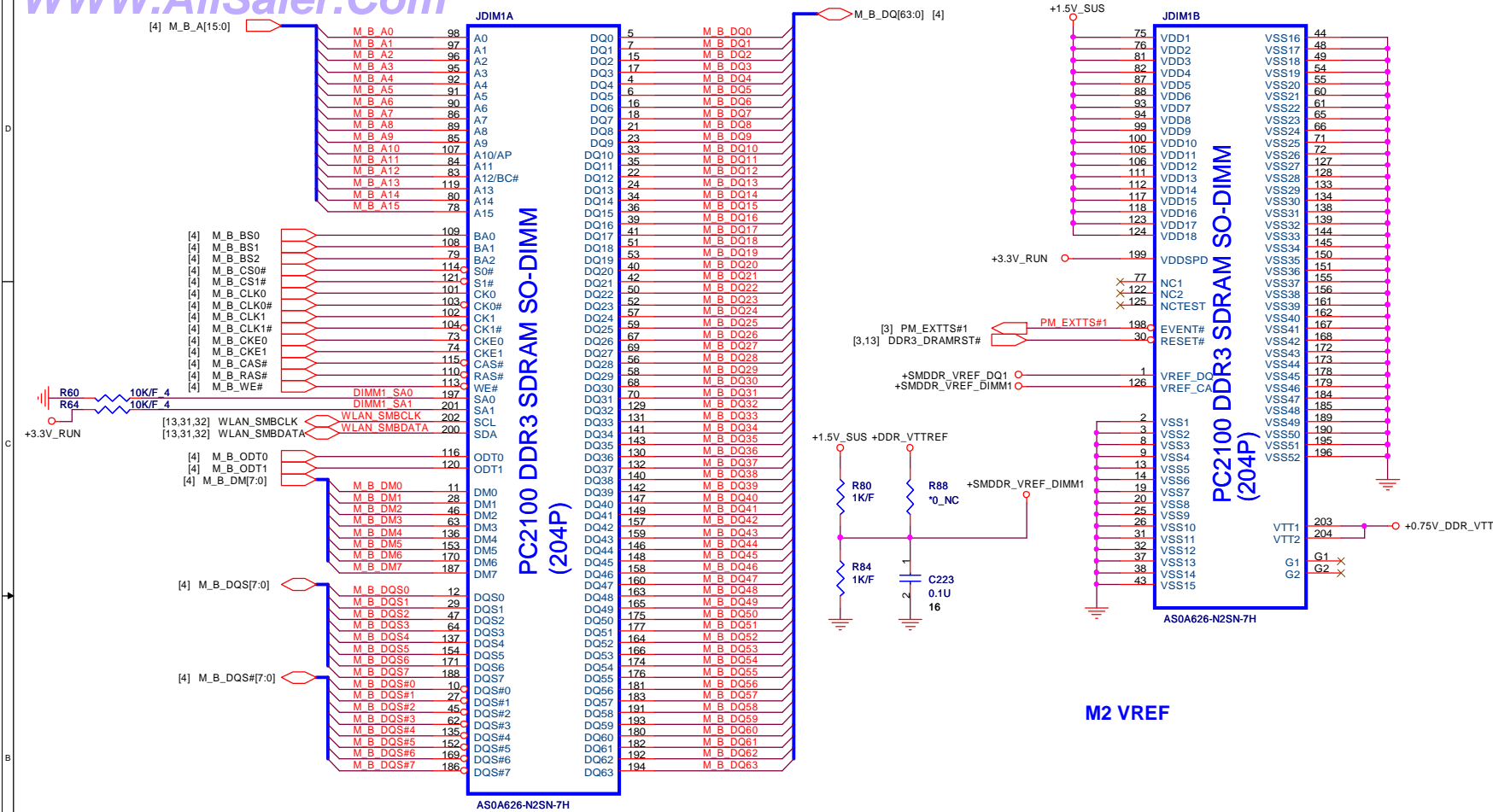
BoxPeak-M\_QMGS



File	IBEX PEAK-M 6/6
Size	Document Number UM3
Date	Thursday, October 15, 2009
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Rev	1A



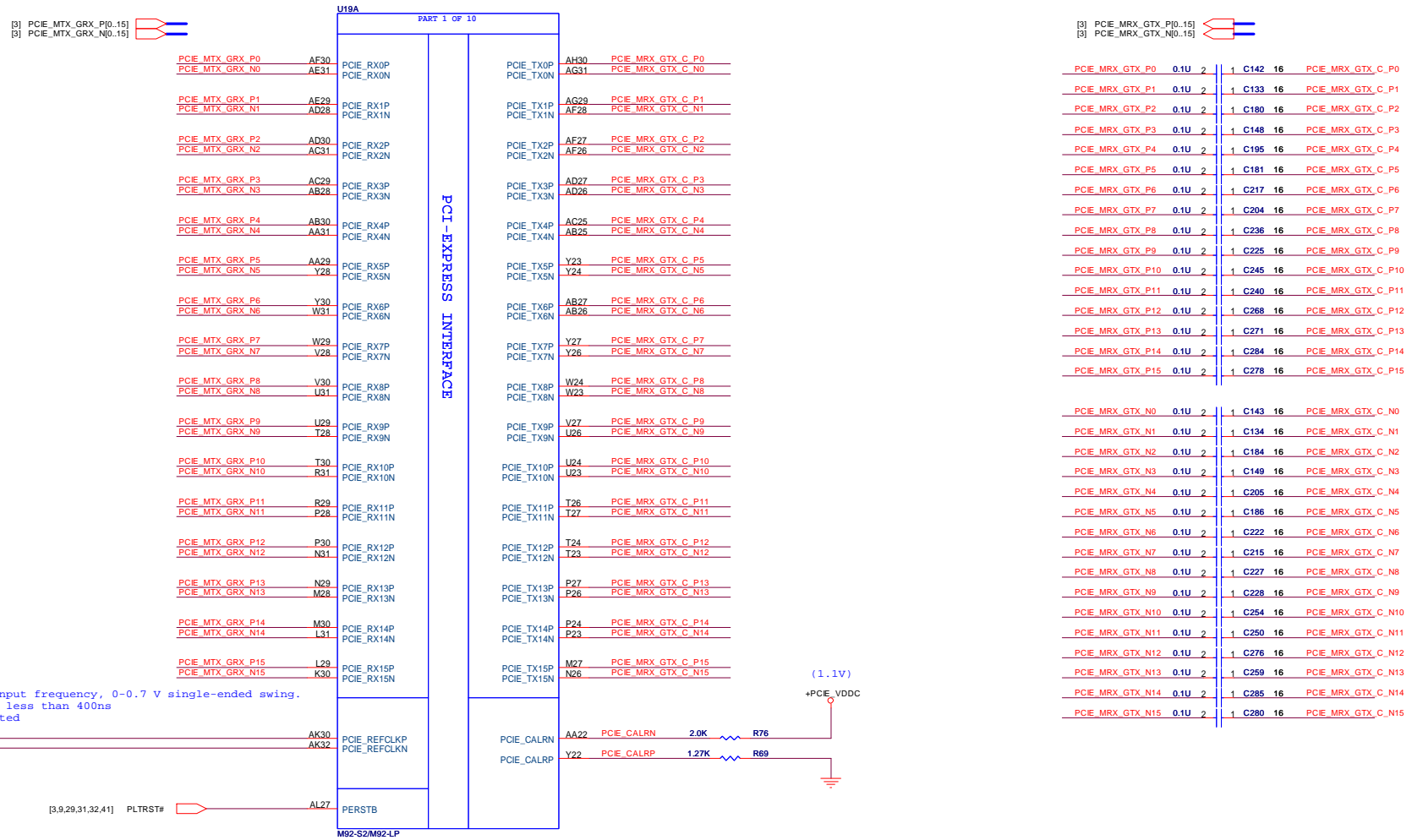
File	DDR3 DIMM-0	Rev	1A
Size	Document Number	UM3	
Date	Thursday, October 15, 2009	Sheet	13 of 63






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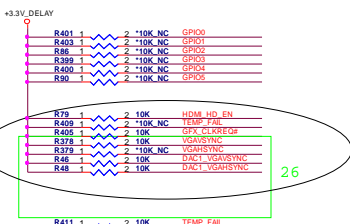
M92-S2 XT AJ072800T04 100-CG1675(216-0728004)  
M92-S2 AJ072800T03 100-CG1643(216-0728003)

 <b>QUANTA COMPUTER</b>		
Title VGA-M92-XT PCIE		
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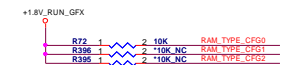
MEMORY APERTURE SIZE SELECT	CF03 GP109	CF02 GP1013	CF01 GP1012	CF00 GP1011
128MB	0	0	0	0
256MB	0	0	0	1
64MB	0	0	1	0
512MB	1	0	0	0



GPIO Straps	DESCRIPTION OF DEFAULT SETTINGS	FM9 setting
GPIO0	GPIO0: TL_PWRSE_EN (Transceiver Power Savings Enable) 0: 50% Tx output swing (for mobile mode) 1: Full Tx output swing (Default setting for Desktop)	0
GPIO1	GPIO1: TL_DEEMPH_EN (Transceiver De-emphasis Enable) 0: 1.5 dB de-emphasis disabled (for mobile mode) 1: 1.5 dB de-emphasis enabled (Default setting for Desktop)	0
GPIO2	GPIO2: BF_GEN2_EN (5.0 GT/s Enable) 0: 5-Step Selectable (Controlled Gen2) 1: 1-Step Selectable (Controlled Gen2)	0
GPIO3	ATI reserved configuration straps.	0
GPIO4	ATI reserved configuration straps.	0
GPIO5	GPIO5: AC_BATT 0: Battery saving mode = 0.0 V 1: AC (Performance mode) = 0.1 V	0
GPIO6	ATI Internal use only	0
HSYNC (A026)	00: No Audio function 01: Audio for DisplayPort only 10: Audio for DisplayPort and HDMI if double in desktop 11: Audio for both DisplayPort and HDMI. HDMI must only be enabled on systems that are legally entitled. It is the responsibility of the system designer to ensure that the system is entitled to support this feature.	0
VSYN (A027)		0



DACL_VGA_VS	HD Audio straps
DACL_VGA_VS	0/0: No audio function
0/1	Audio for DisplayPort only
1/0	Audio for DisplayPort and HDMI if double in desktop
1/1	Audio for both DisplayPort and HDMI

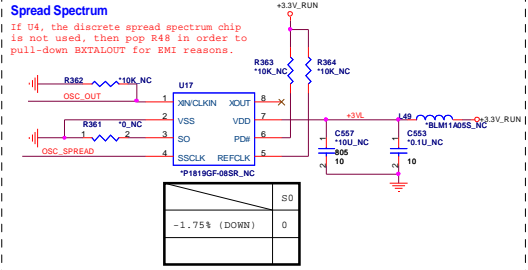
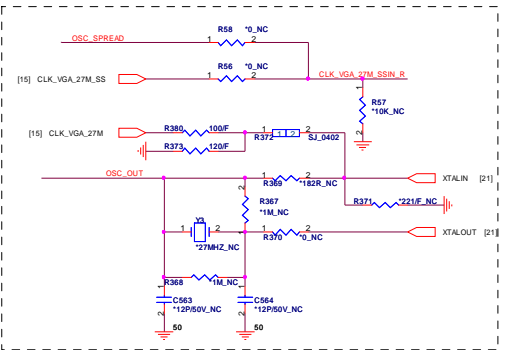


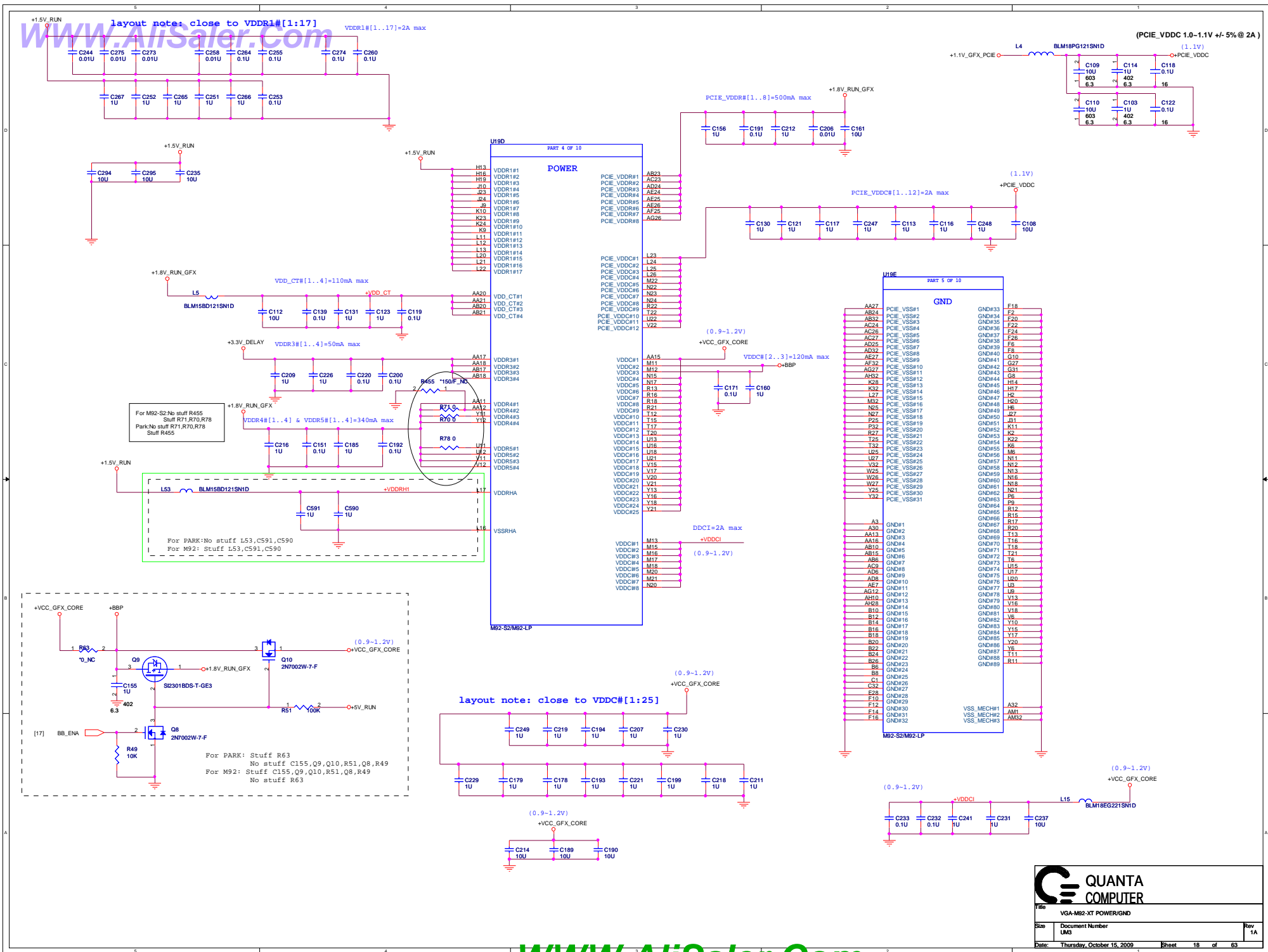
Memory Straps	RAM_TYPE CFG2	RAM_TYPE CFG1	RAM_TYPE CFG0	Quanta PN (QuantaBuy)	Quanta PN (WinBuy)	Vendor PN	31 level PN
800MHz	0	0	0	AKD5LGT502		K4W1G1646B-HC12	
512MB(64M*16) Samsung	0	0	1	AKD5LGT502		K4W1G1646B-HC12	
800MHz	0	1	0	AKD5LGTW00		H5TQ1G63BFR-12C	
512MB(64M*16) Hynix	0	1	0	AKD5LGTW00		H5TQ1G63BFR-12C	



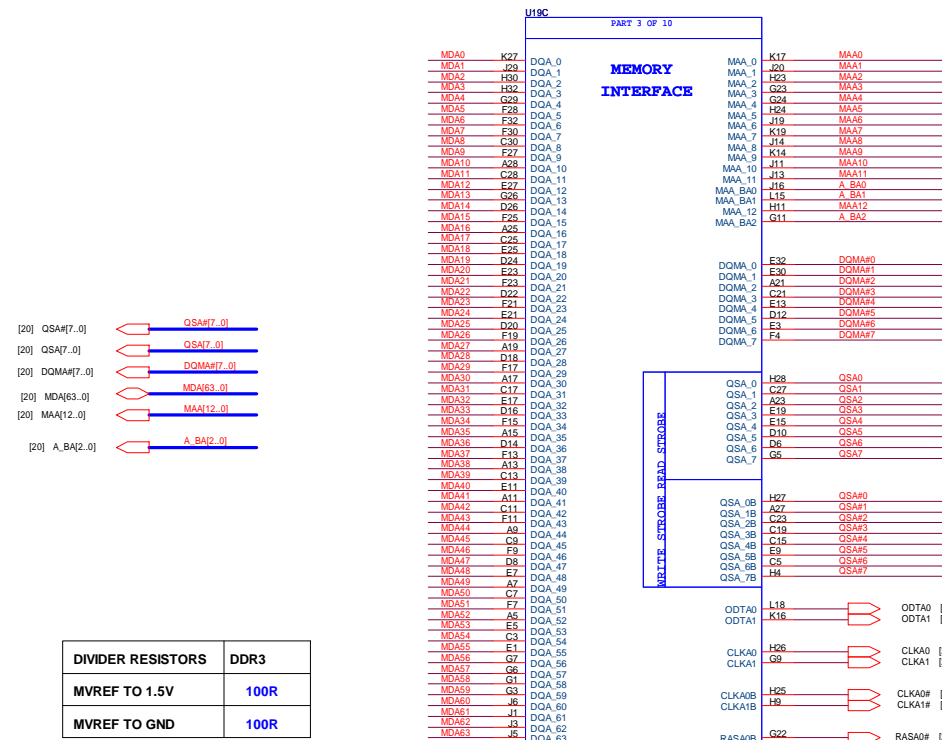
For Park S3:  
Install All components in this Box  
R402, R397, R398, L9, C136, L19, C261

For M92-S2: DO NOT Install any Component  
in this Box.

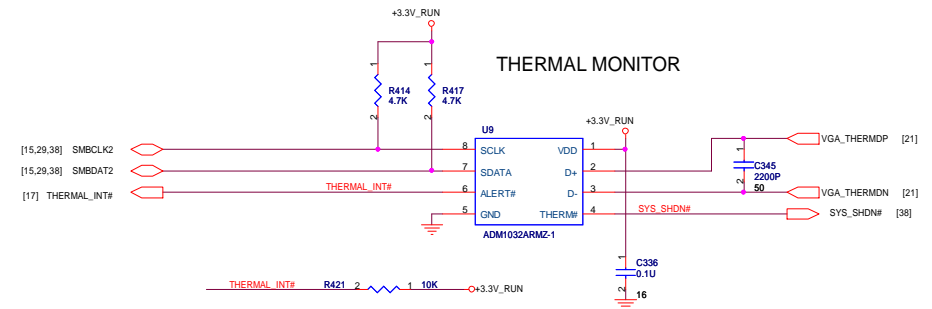
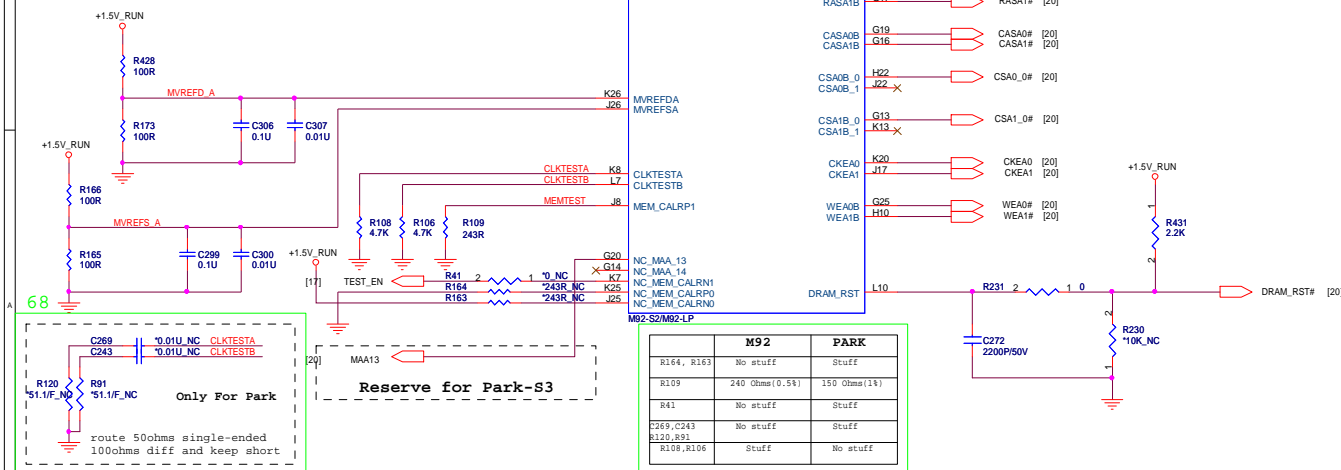




## MEMORY INTERFACE



DIVIDER RESISTORS	DDR3
MVREF TO 1.5V	100R
MVREF TO GND	100R



Change BOM  
Change U7003 from AL001032001 to AL001032002

	M92	Park
R230	No stuff	Stuff
R231	0 ohm PN:CS00002JB38	680 ohm PN:CS16802FB01
R431	Stuff	No stuff
C272	2200pF PN:CH2226K9B00	68pF PN:CH06806JB01



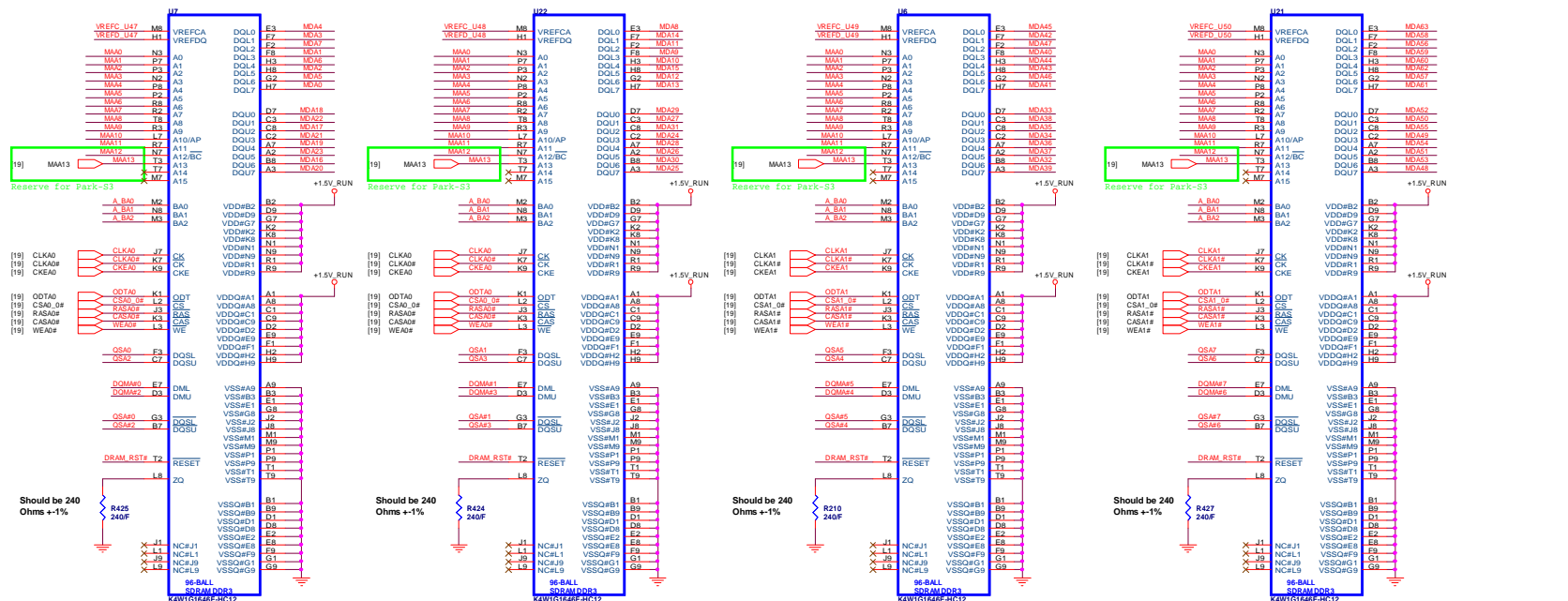
Title VGA-M92-XT MEMORY/THERM

Size	Document Number UM3
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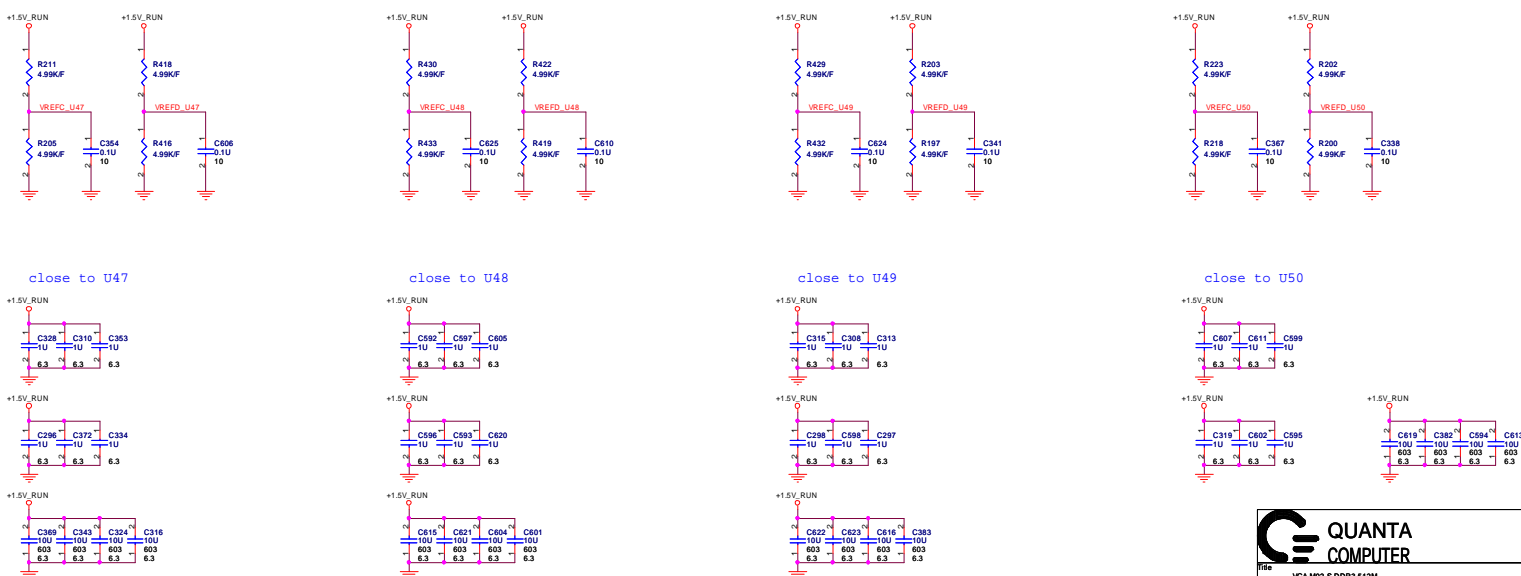
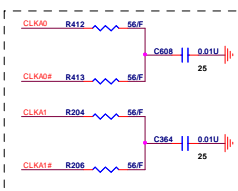
Date: Thursday, October 15, 2009 Sheet 19 of 63

- [19] MDMA3.0) MMA13.0)
- [19] MA12.0) MMA12.0)
- [19] QSA7.0) QSA7.0)
- [19] QSA7.0) QSA7.0)
- [19] QDMA7.0) QDMA7.0)
- [19] DRAM\_RST# DRAM\_RST#
- [19] A\_BA2.0) A\_BA2.0)

## DDR3

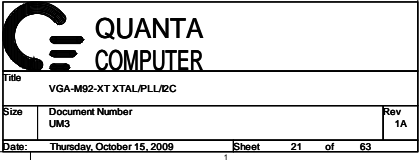


Placement has to be close to VRAM

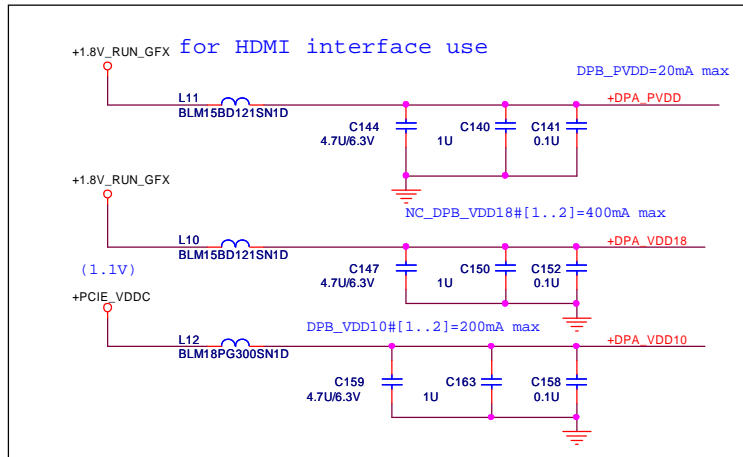
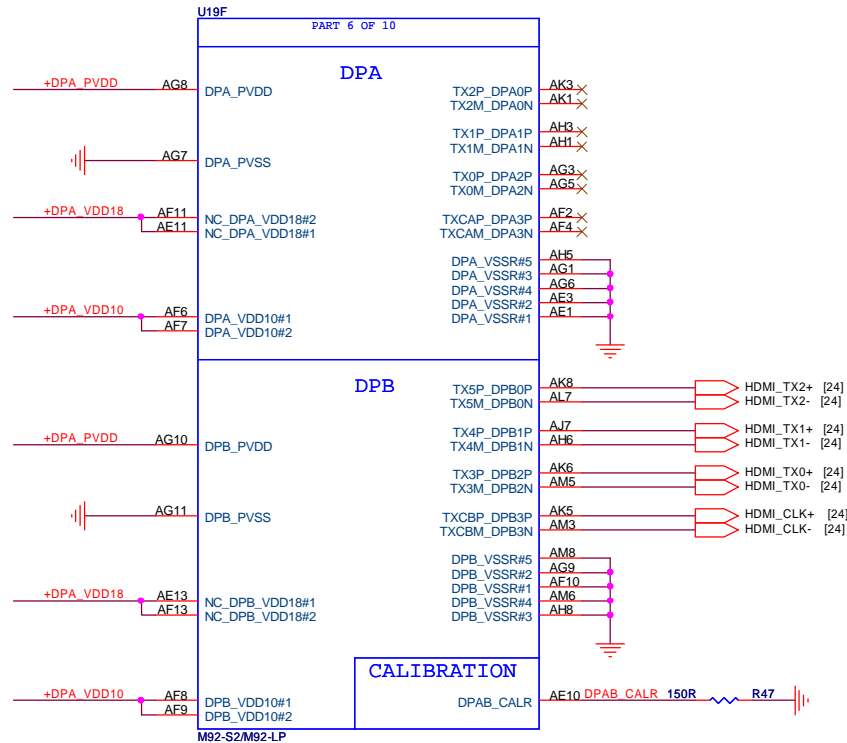


QUANTA COMPUTER

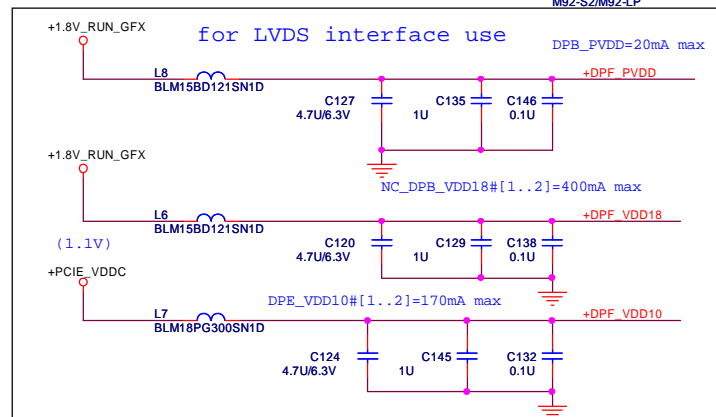
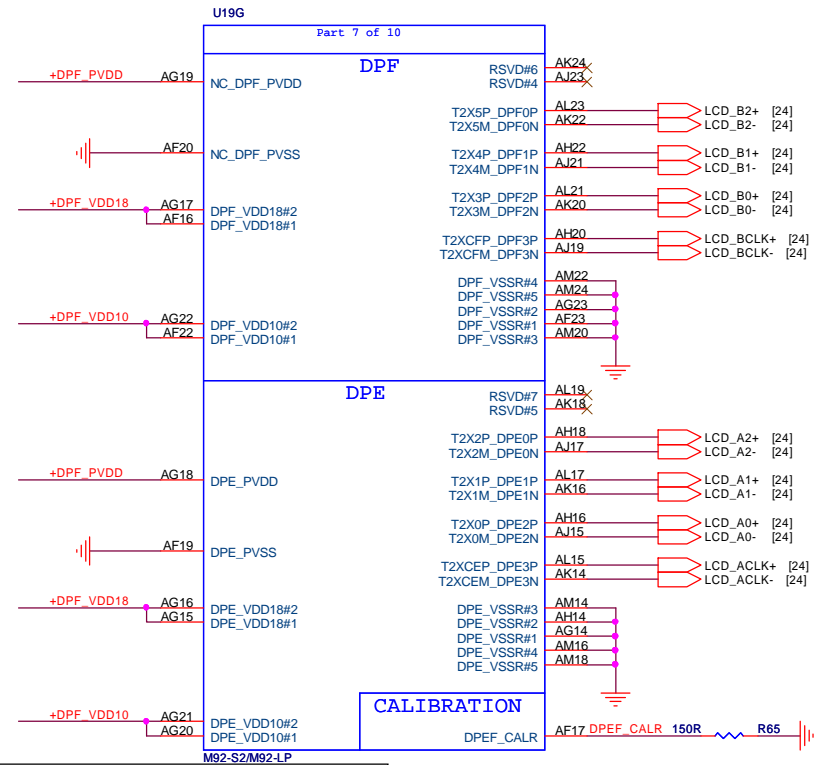
Rev 1A



# TMDP(HDMI) INTERFACE




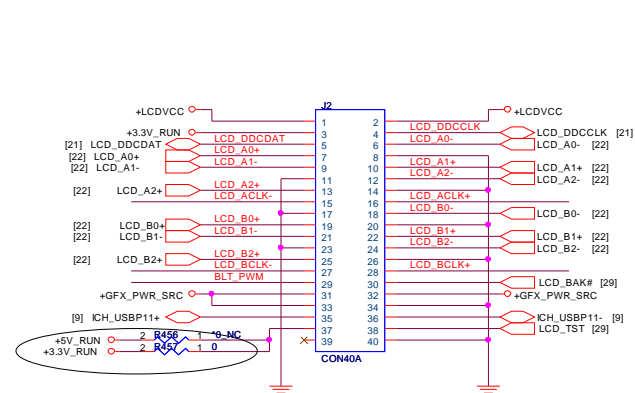
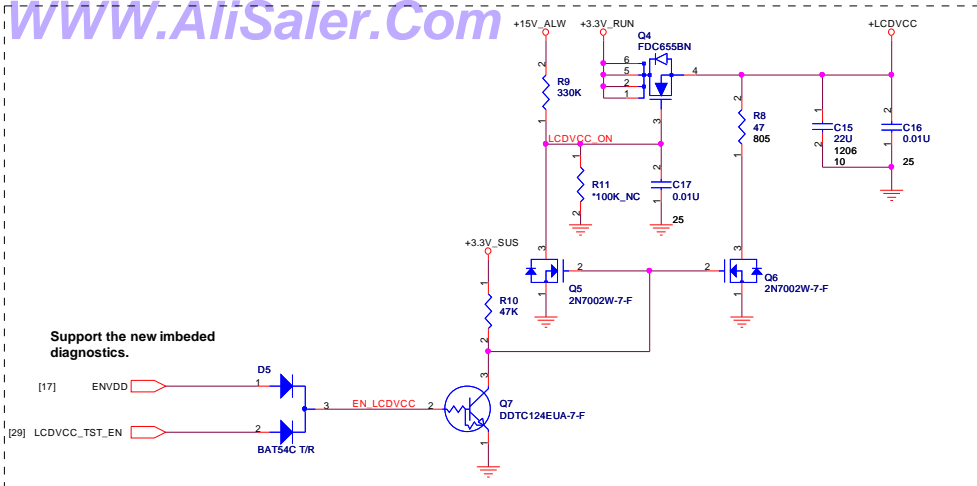
# LVDS INTERFACE



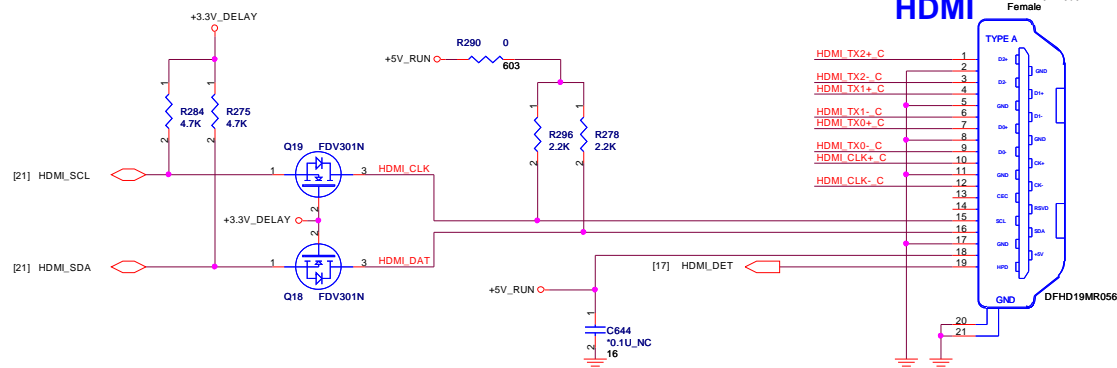
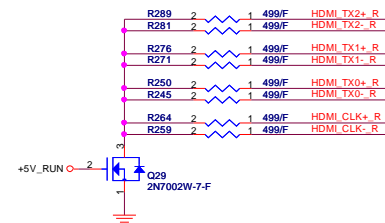
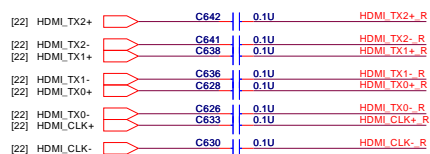
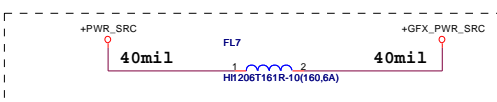
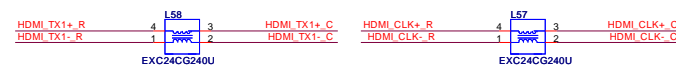
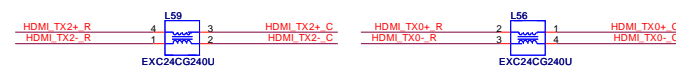
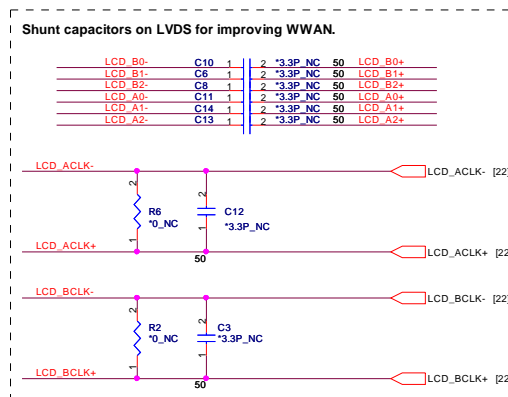
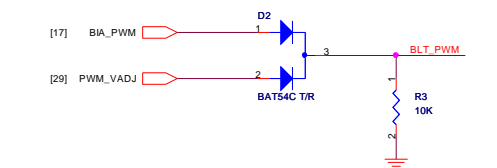
QUANTA COMPUTER		
Title VGA-M92-XT TMDP I/F		
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Title Blank Page			
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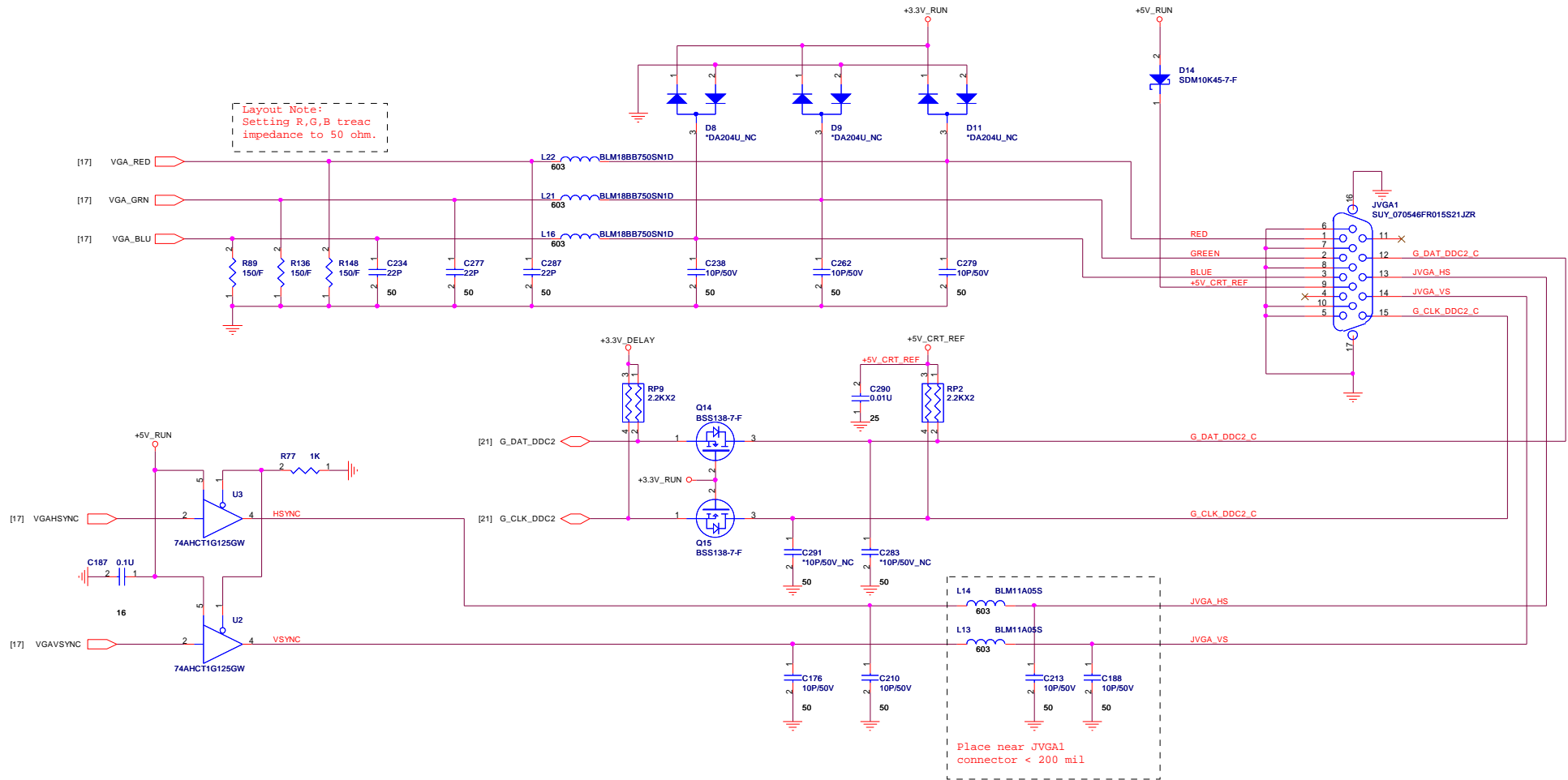
Need to check  
DFWF40MR000

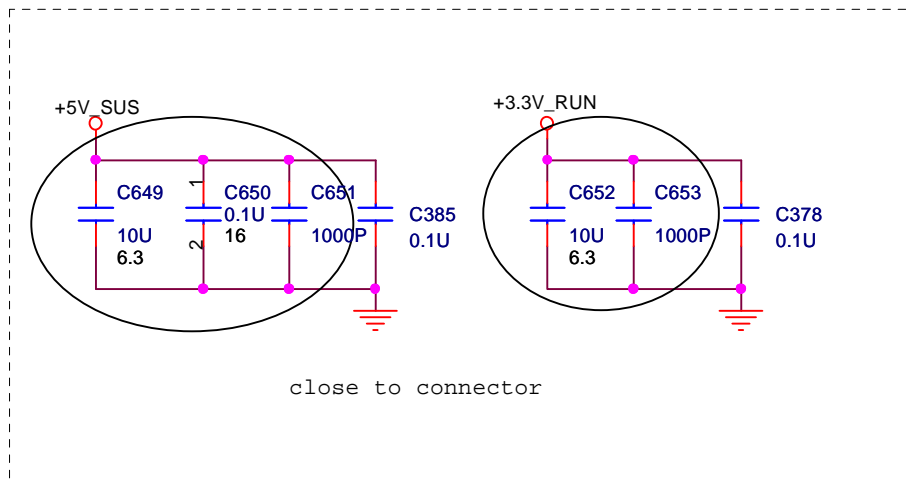
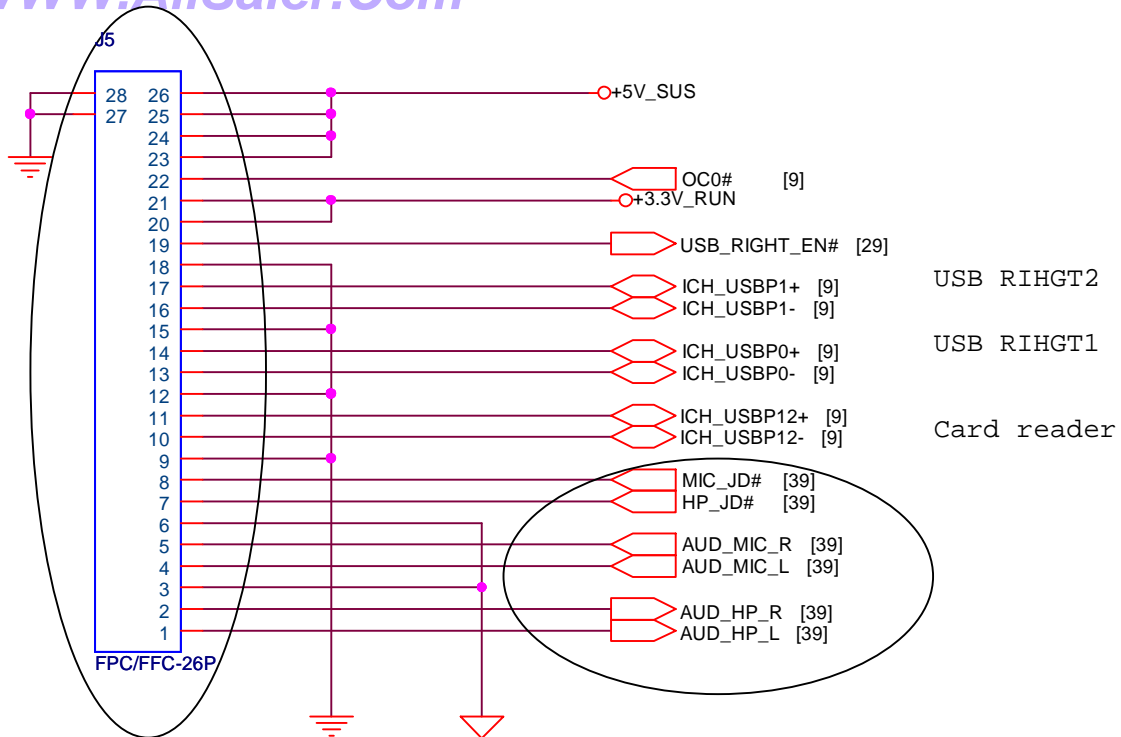



DFHD19MR056




Title			
LCD CONN / HDMI CONN			
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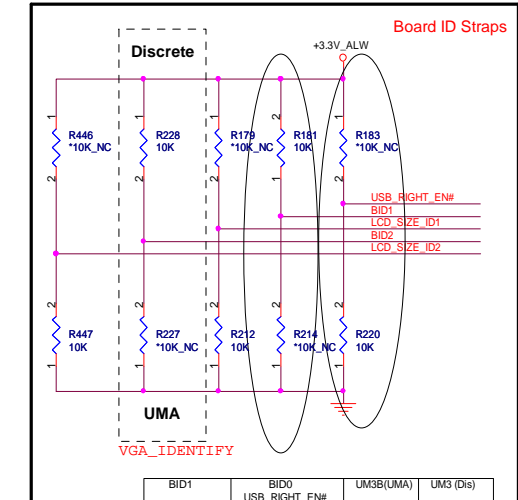
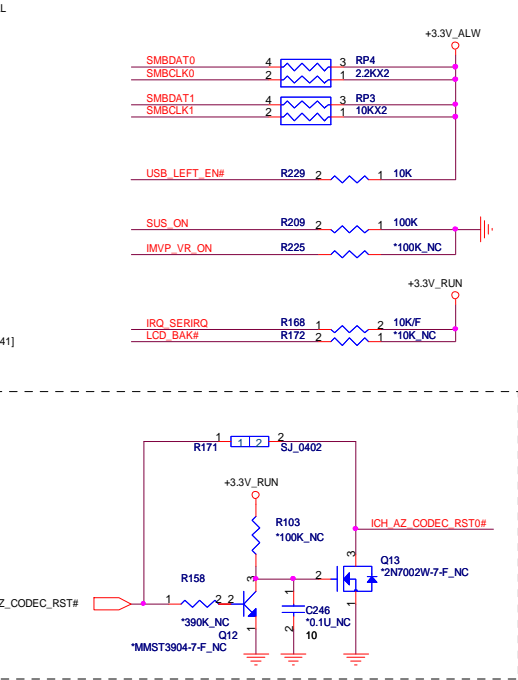
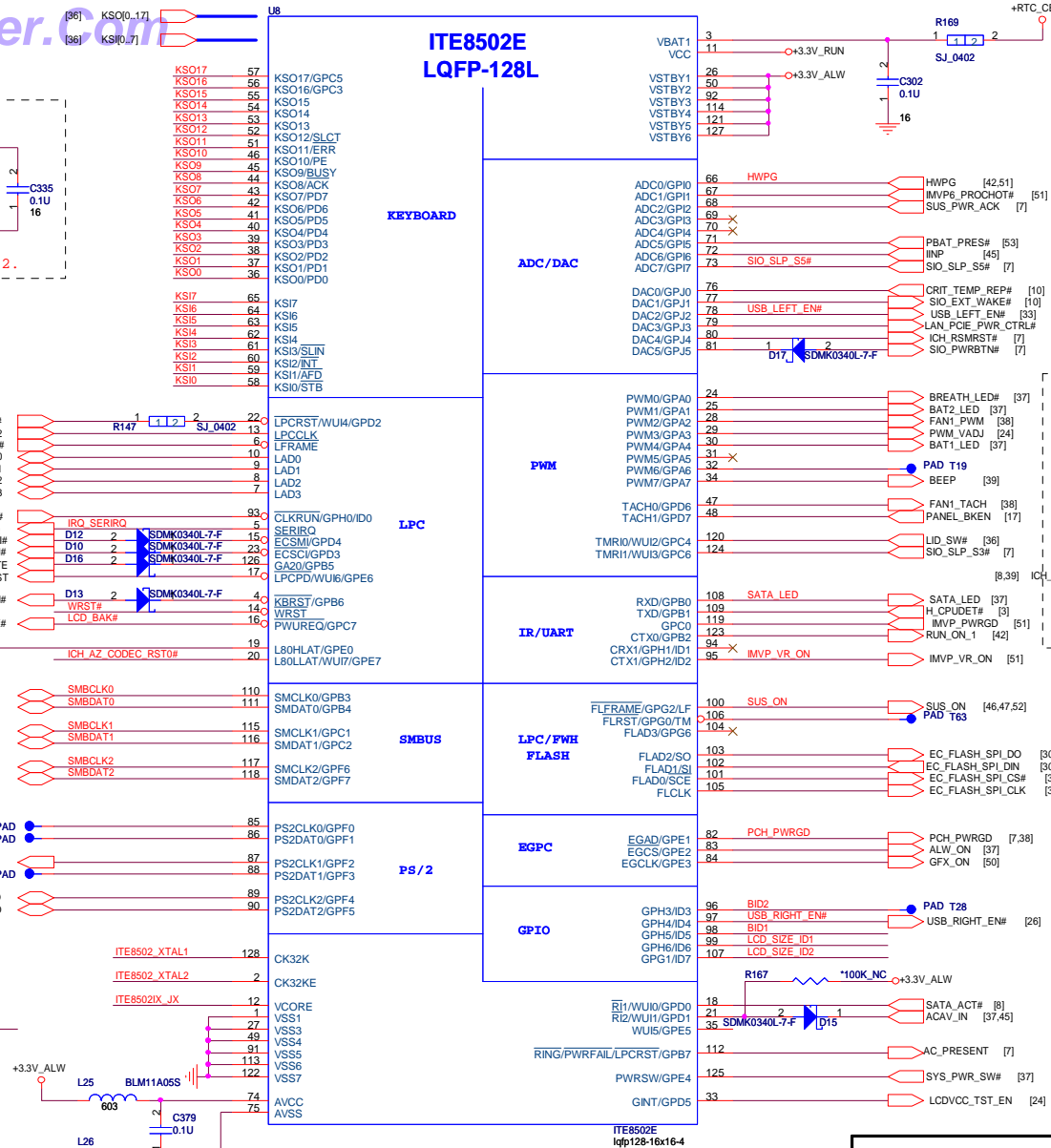
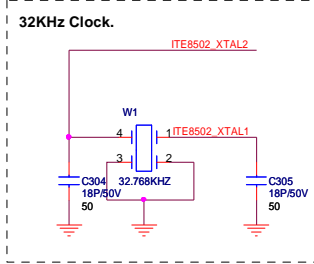
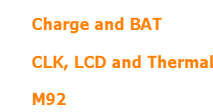
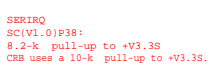
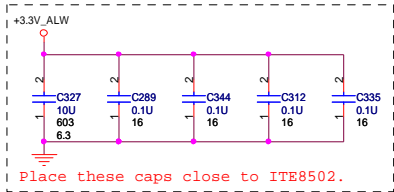


 <b>QUANTA COMPUTER</b>		
Title DB CONN		
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QUANTA  
COMPUTER

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Title Blank Page			
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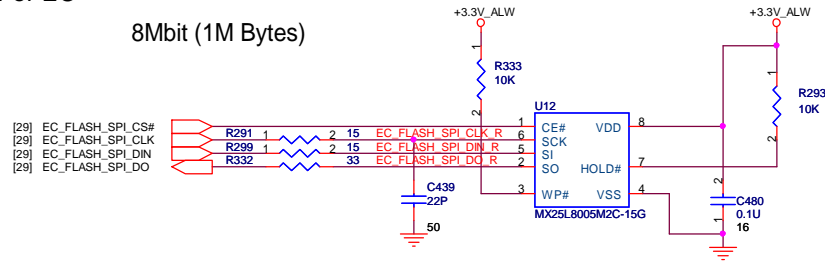


	LCD_SIZE_ID1 (99)	LCD_SIZE_ID2 (107)	0	0	SSI (X00) PT (X01)	SSI (X00) PT (X01)
14"	0	0	1	0	ST (X02)	ST (X02)
15.6"	1	0	1	1	QT (A00)	QT (A00)
17"	0	1	0	0	(A01)	(A01)



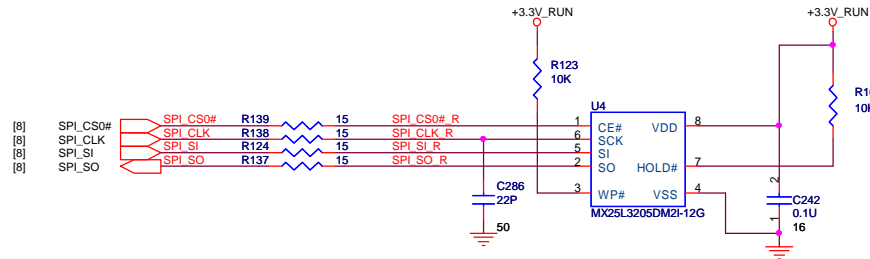
For EC

8Mbit (1M Bytes)

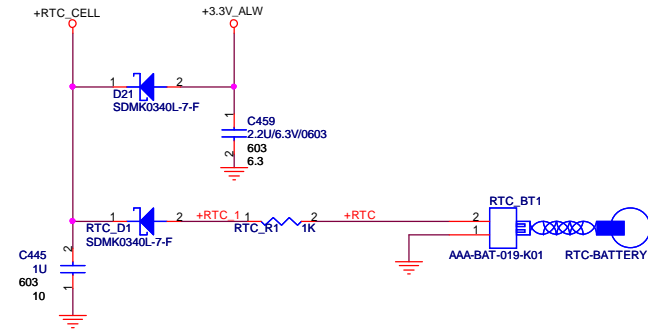


For PCH

32Mbit (4M Bytes)



RTC BATTERY



Title: FLASH/RTC

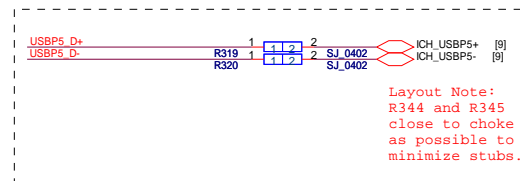
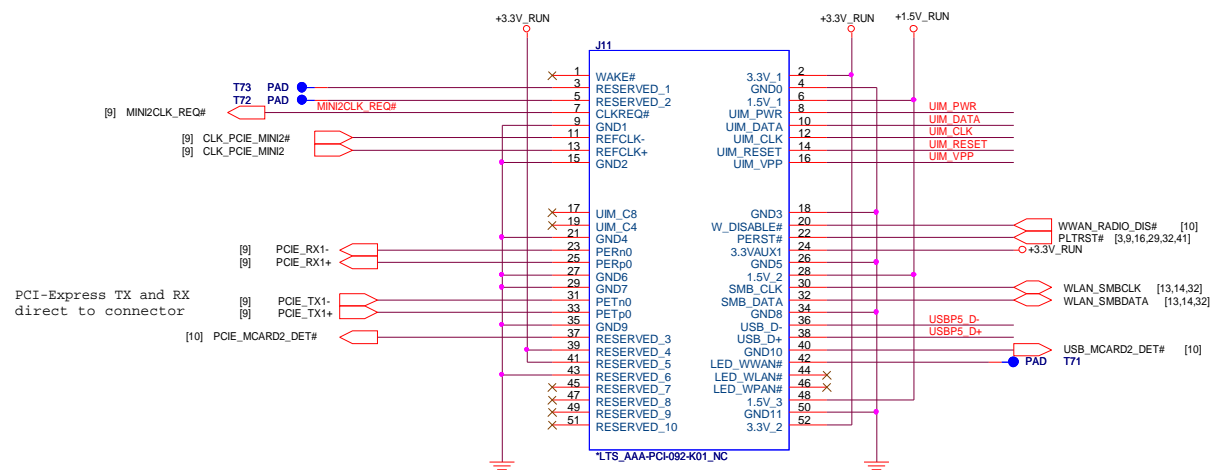
Size: Document Number UM3

Date: Thursday, October 15, 2009

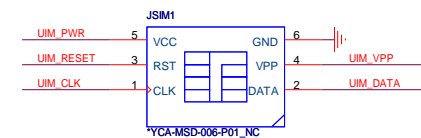
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# MiniCard WWAN connector

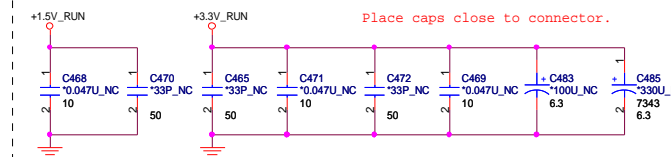
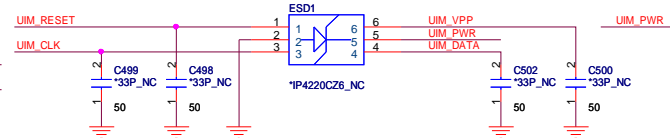


Layout Note:  
R344 and R345  
close to choke  
as possible to  
minimize stubs.



Place as close as possible to JSIM1 connector

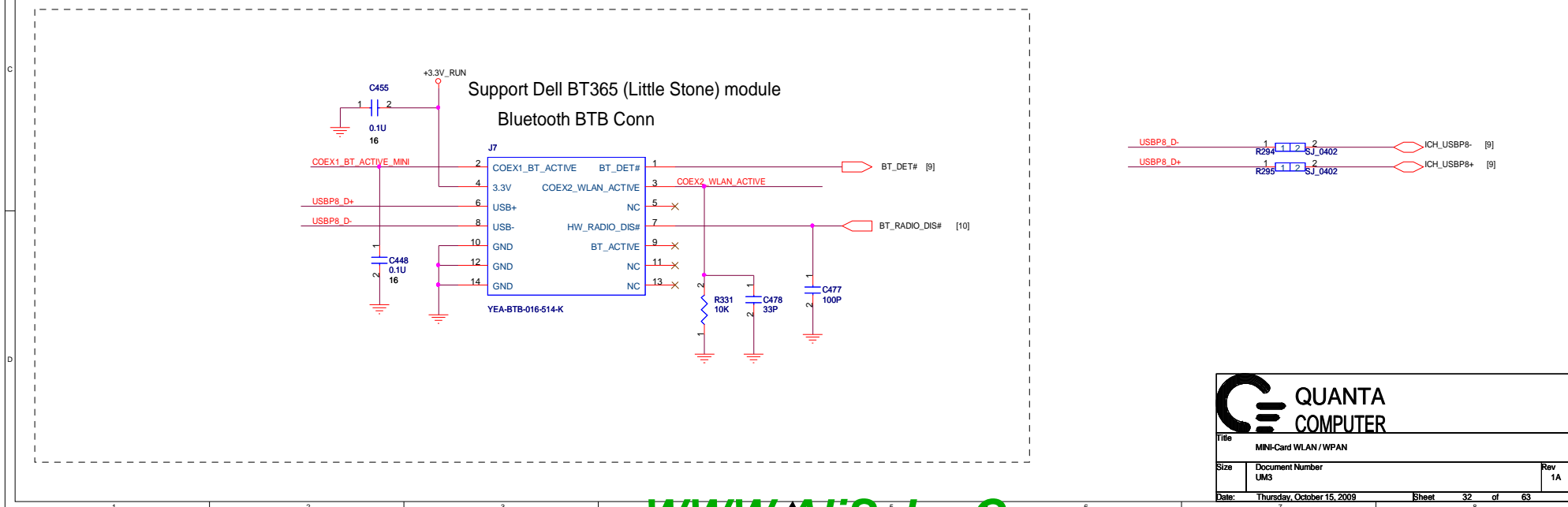
DFHS06FR043



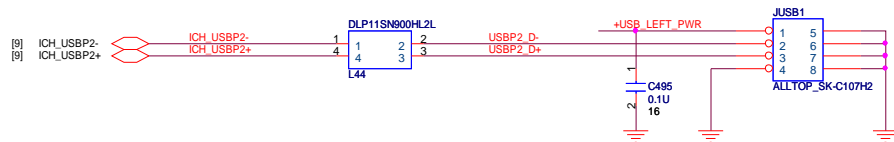
Place caps close to connector.



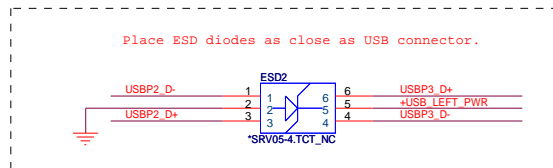
Title		
MINI-Card WWAN		
Size	Document Number	Rev
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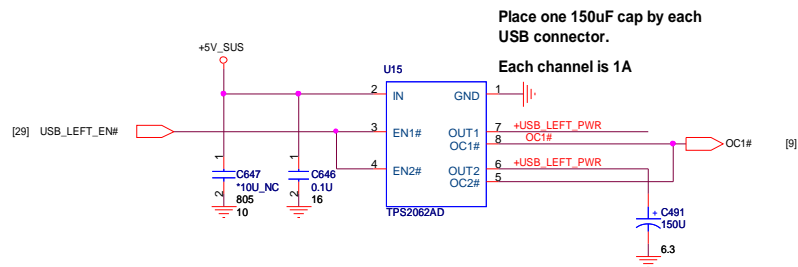
External USB PORT hookup reference. Your design may need more or less external ports and may be mapped differently



Platforms should put in PADS for the USB chokes if they have the room. Chokes should be NOPOP.



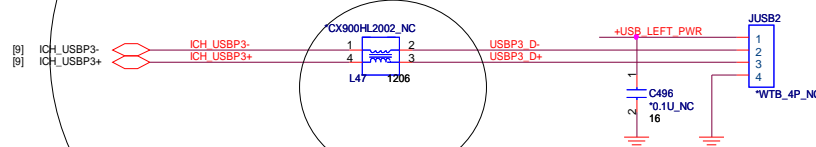
Place ESD diodes as close as USB connector.




Place one 150uF cap by each USB connector.  
Each channel is 1A

REV FOR 17"

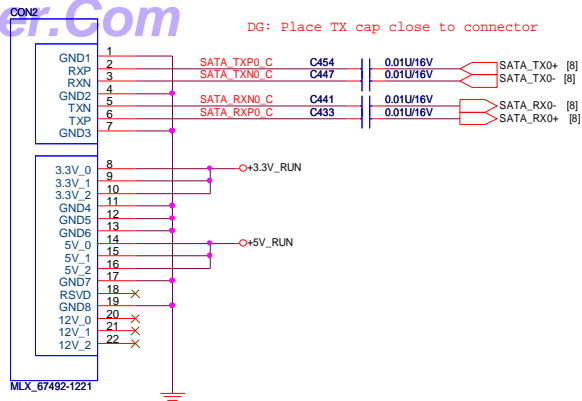
Add L47 ,C496 , JUSB2 for UM5



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Title Blank Page			
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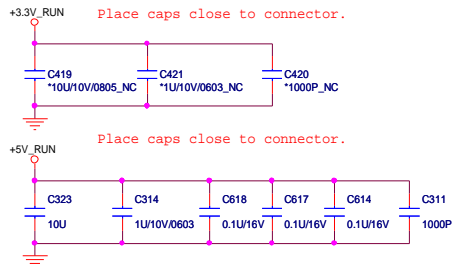
# SATA Connector.



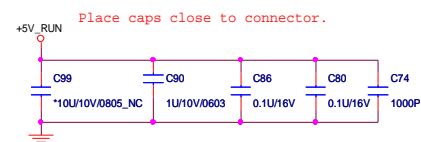
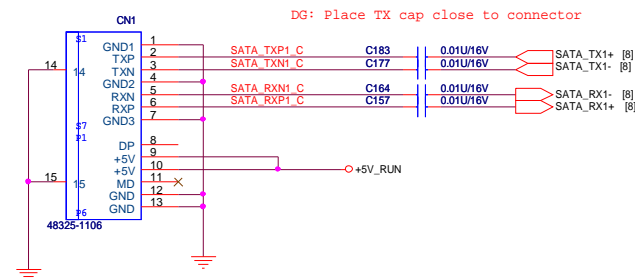
UM5與UM3/6不同，只差在高度，footprint沒變

UM5/UM5B  
PN:DFHS22FR137  
Mfr:67492-1224

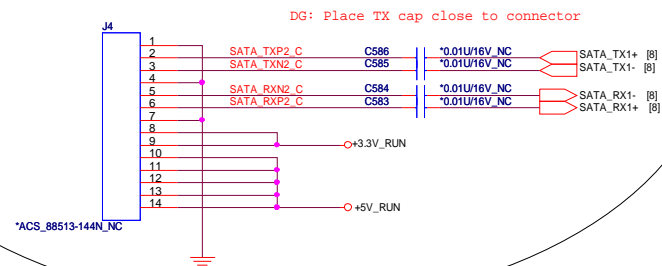
UM3/UM3B/UM6/UM6B  
PN:DFHS22FR0B2  
Mfr:67492-1921



## ODD Connector



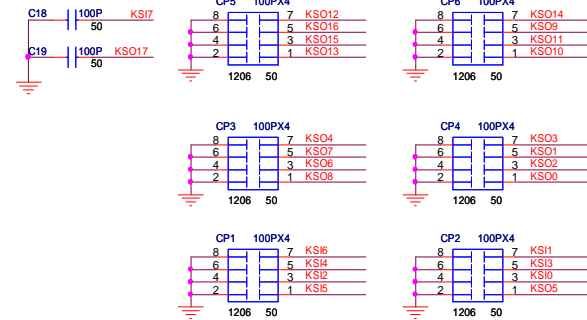
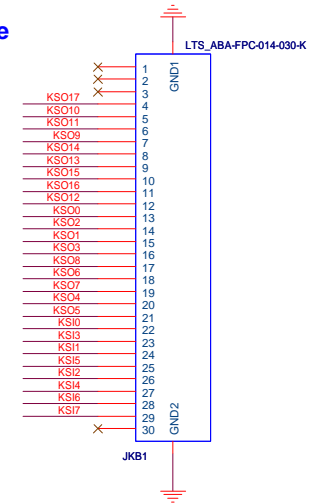
REV FOR 15.6"



# KEYBOARD CONNECTOR

Top side

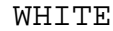
[29] KSO[0..17]  
[29] KSI[0..7]



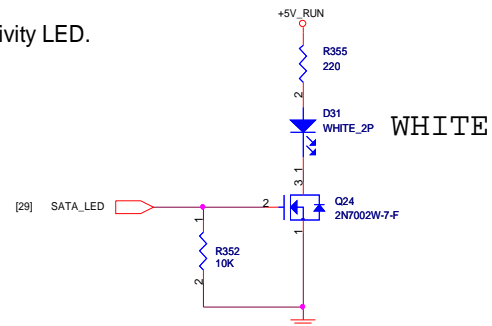
100P CAPS CLOSE TO JKB1

<b>QUANTA COMPUTER</b>		
Title: TOUCH PAD, KB		
Size:	Document Number: UMS	Rev: 1A
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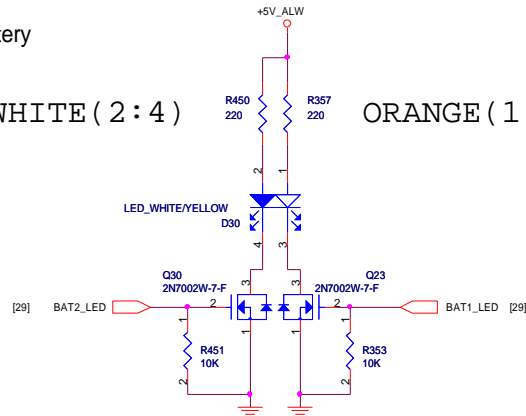


## WHITE

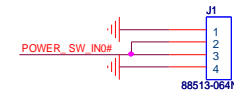


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WHITE( 2:4 )
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ORANGE ( 1 : 3 )

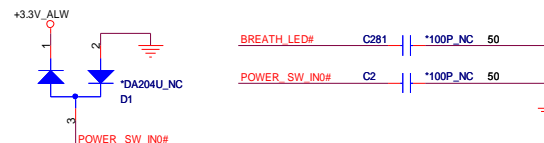
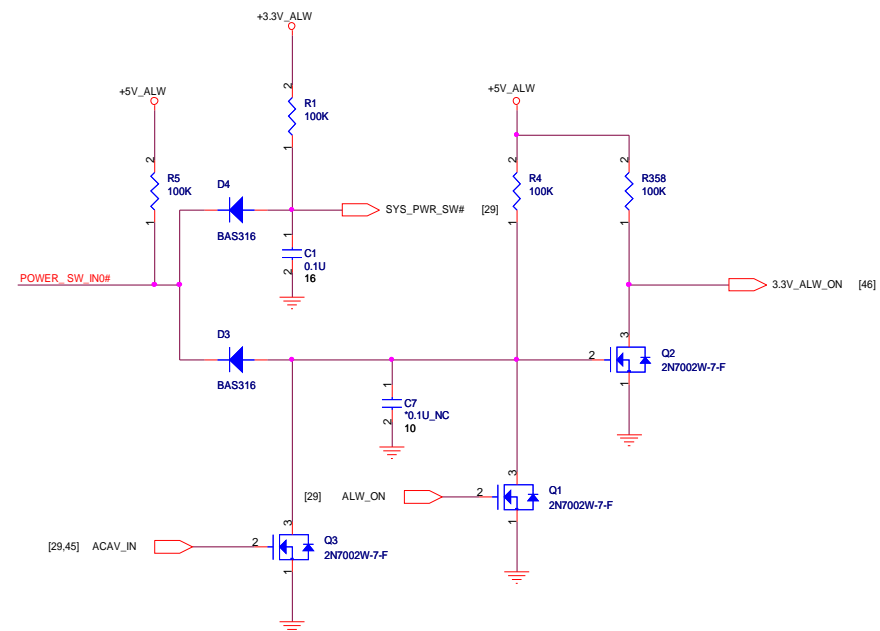


Stephen 7/31



DFFC04FR014

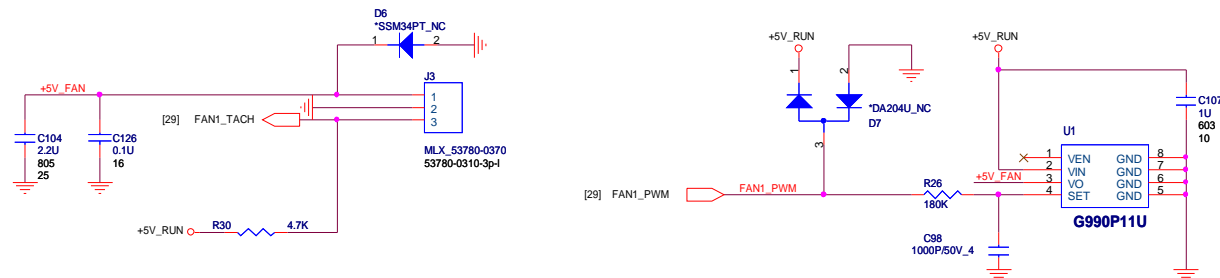
## 3VALW ON POWER LOGIC



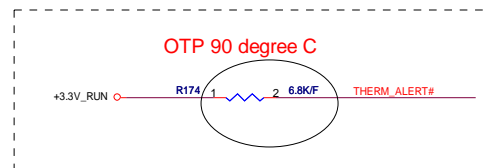
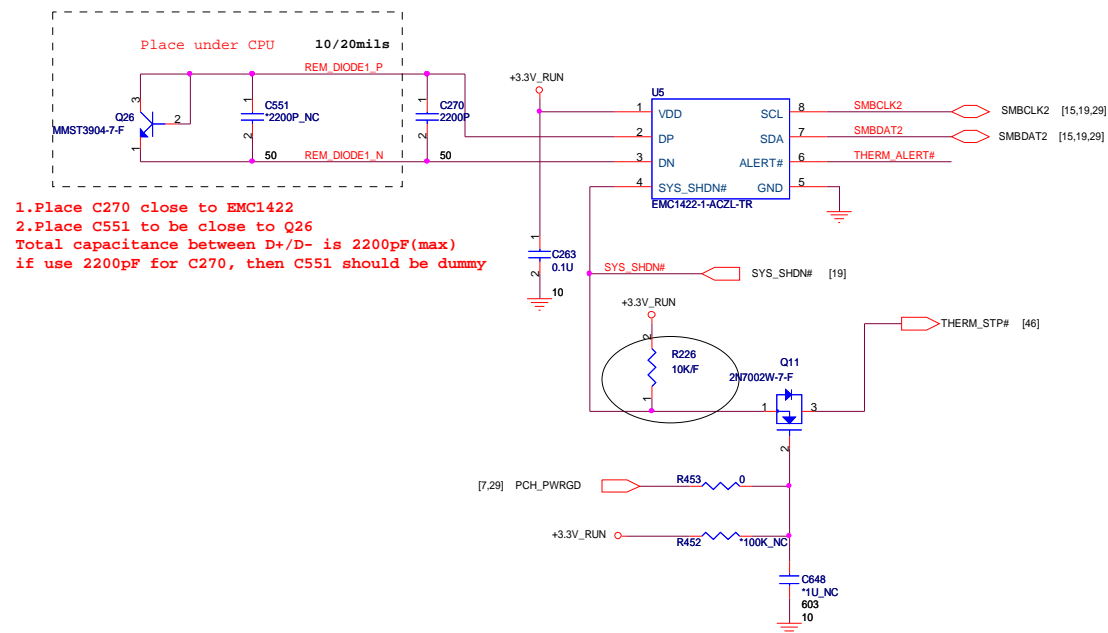
Size	Document Number	Rev
	UM3	1A

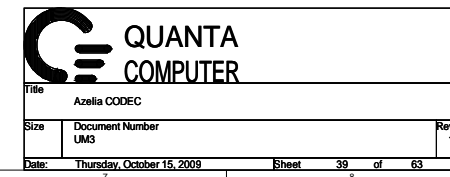
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## FAN CONTROL



Thermal sensor

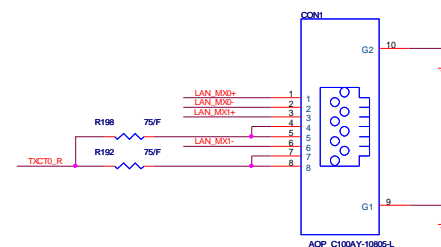




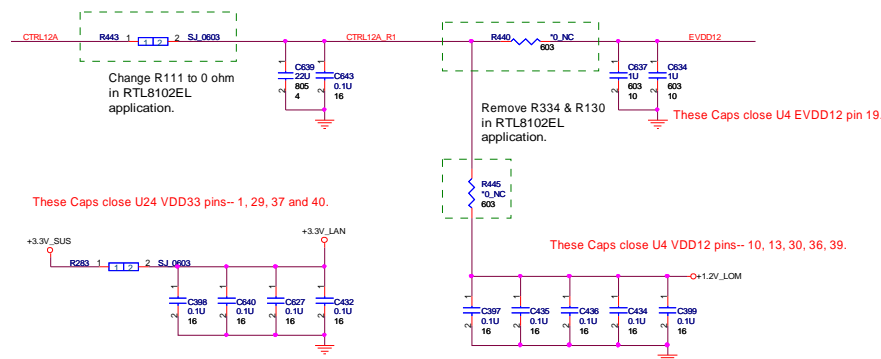


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COMPUTER

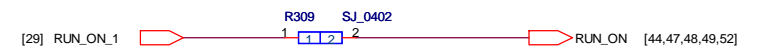
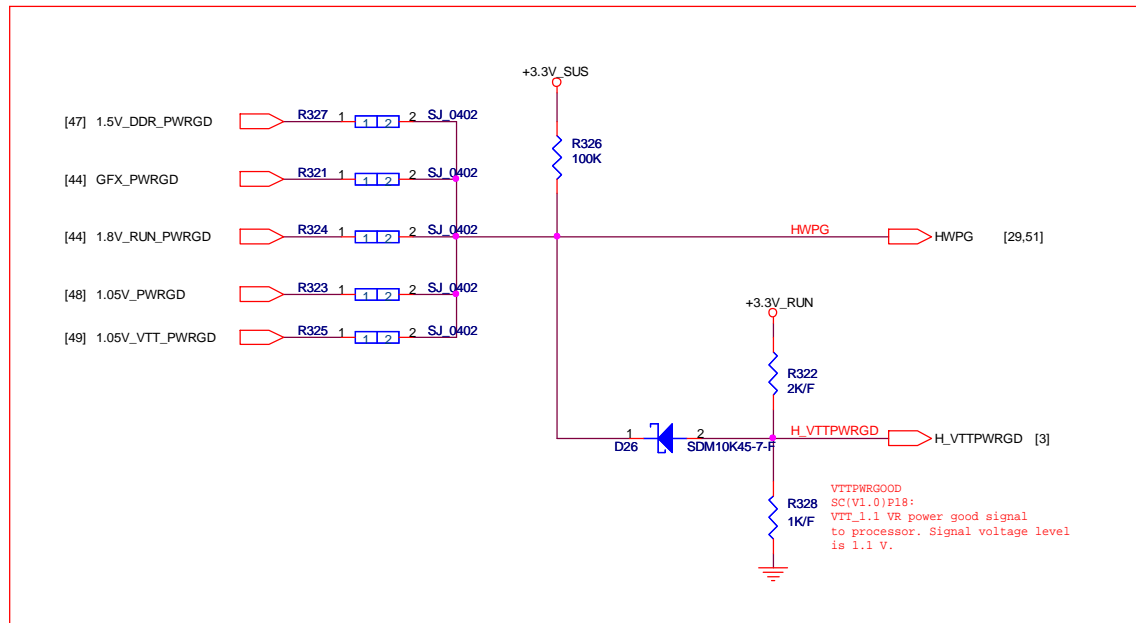
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[9]	CLK_PCIE_LOM		CLK_PCIE_LOM				
[9]	CLK_PCIE_LOM#		CLK_PCIE_LOM#				
[9]	PCIE_RX6+/GLAN_RX+		C632	0.1U	10	LAN_PCIE1XP	
			C629	0.1U	10	LAN_PCIE1XDN	
[9]	PCIE_TX6+/GLAN_TX+		PCIE_TX6+/GLAN_TX+				
			PCIE_TX6-/GLAN_TX-				




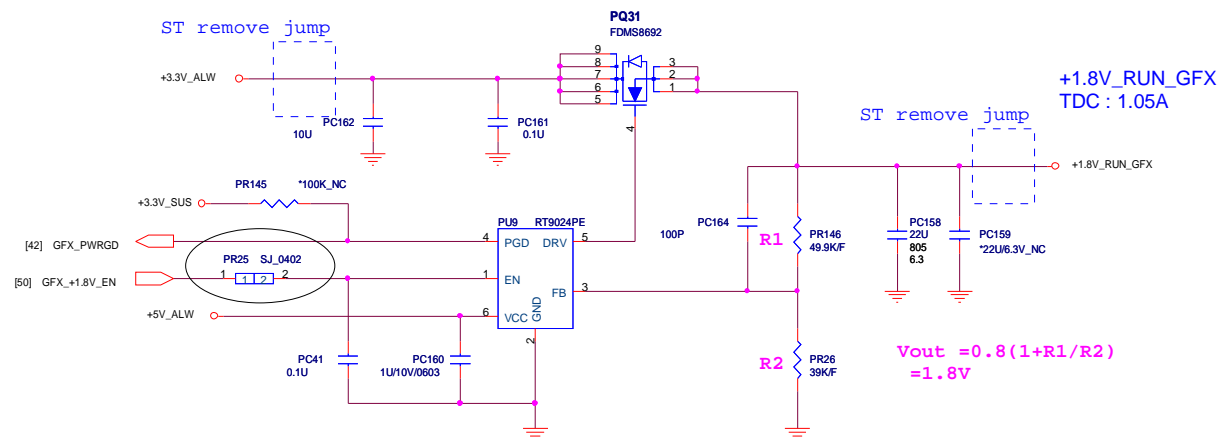
These Caps close U4 VDD12 pins-- 10, 13, 30, 36, 39.



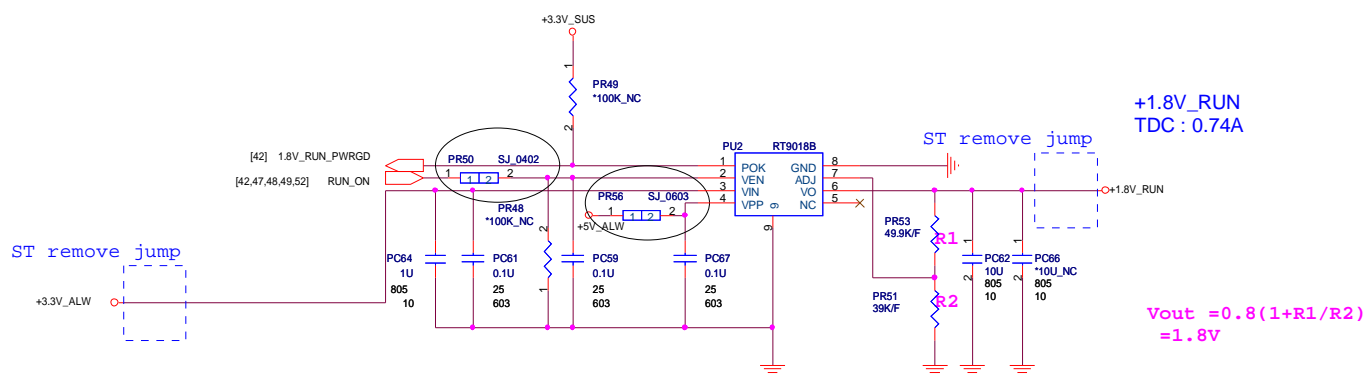
 <b>QUANTA COMPUTER</b>			
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1	2	3	4	5
A				A
B				B
C				C
D				D

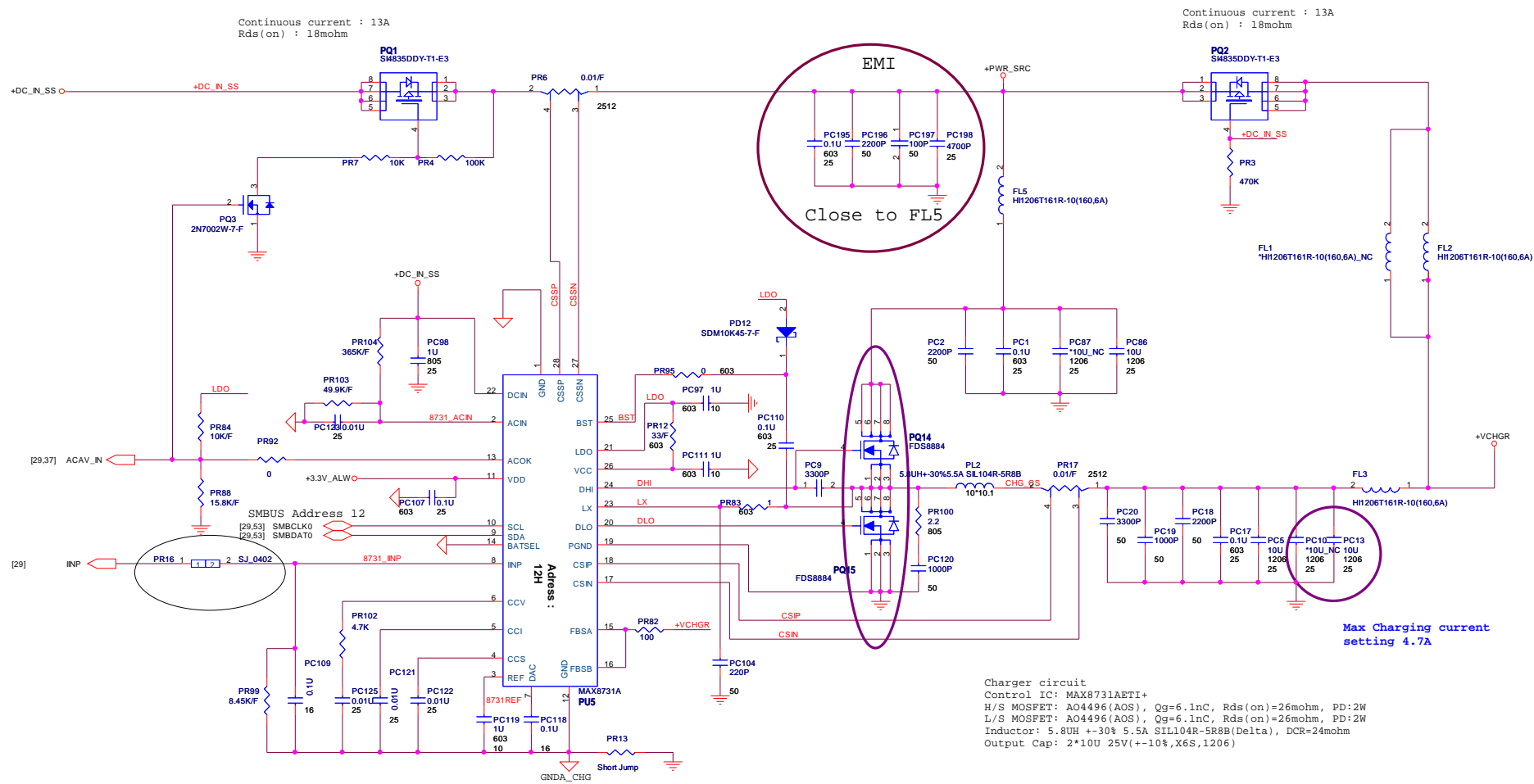
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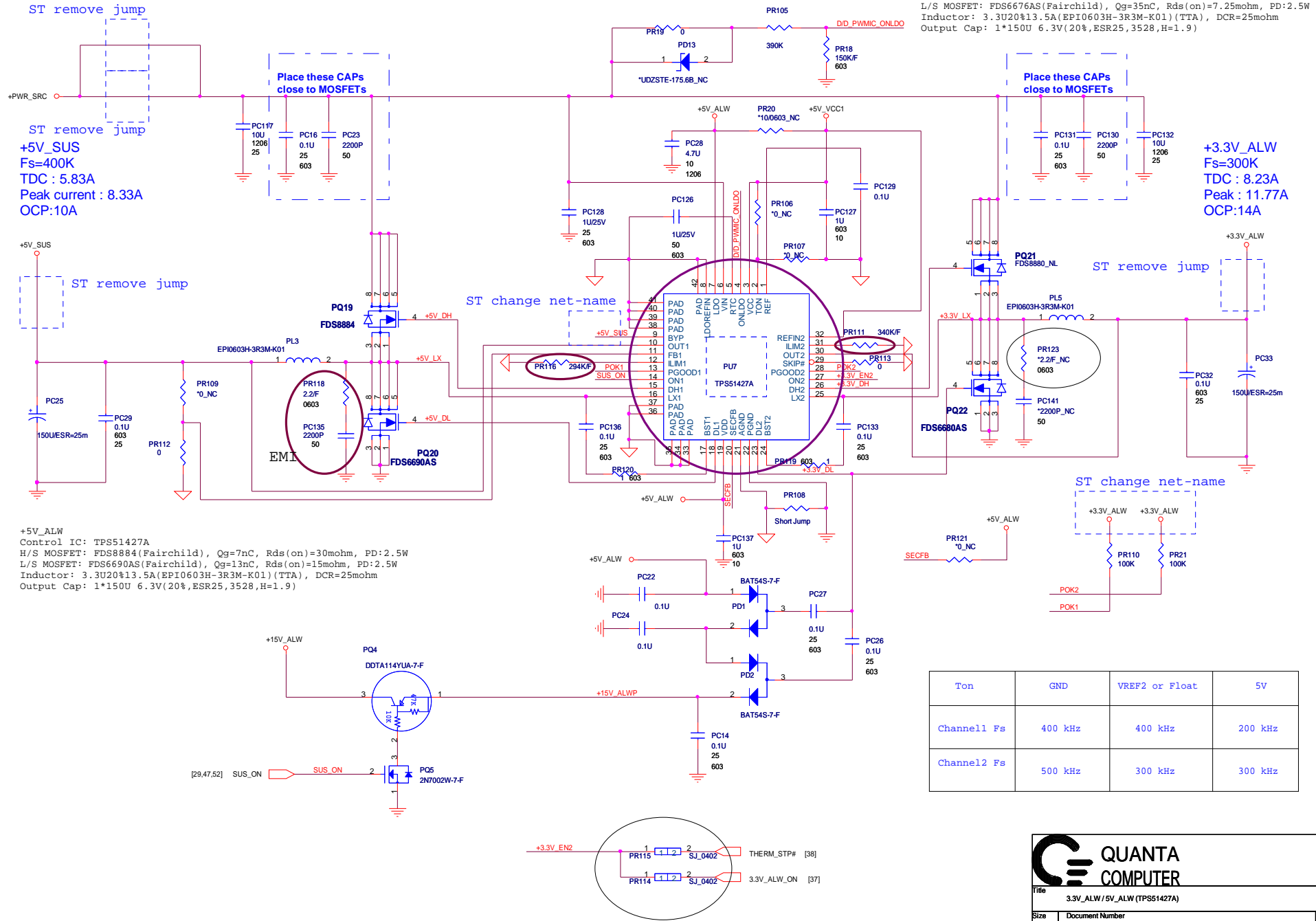
+1.8V\_RUN\_GFX for VGA 1.8V  
+1.8V\_RUN for CPU and PCH 1.8V







Charger circuit  
Control IC: MAX8731AETI+  
H/S MOSFET: A04496(AOS), Qg=6.1nC, Rds(on)=26mohm, PD=2W  
L/S MOSFET: A04496(AOS), Qg=6.1nC, Rds(on)=26mohm, PD=2W  
Inductor: 5.0uH +30% 5.5A S1104R-5R8B(Delta), DCR=24mohm  
Output Cap: 2\*10u 25V(+10%, X6S,1206)

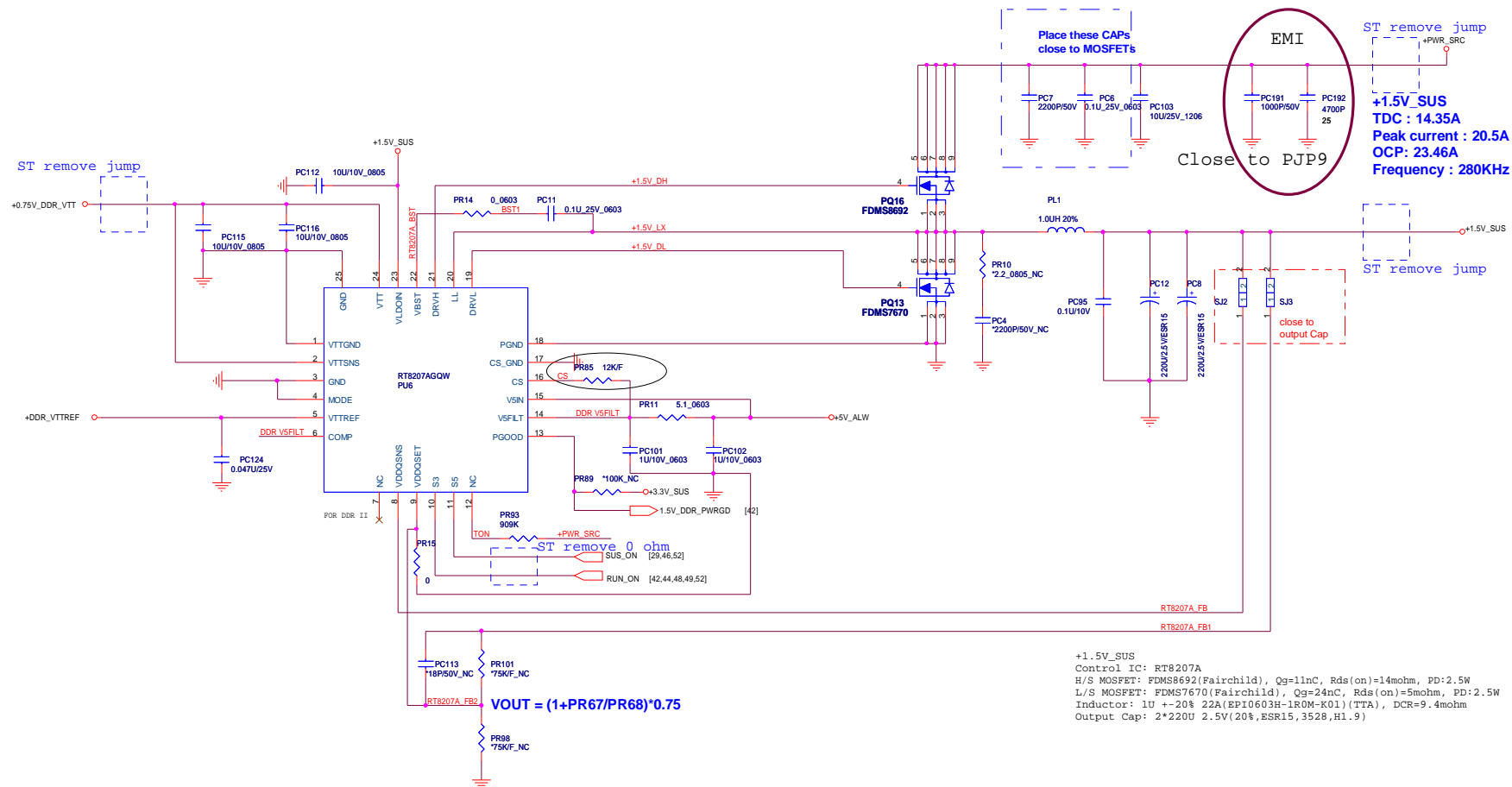


+3.3V\_ALW  
Control IC: TPS51427A  
H/S MOSFET: FDS6298(Fairchild), Qg=14nC, Rds(on)=12mohm, PD:3W  
L/S MOSFET: FDS6676AS(Fairchild), Qg=35nC, Rds(on)=7.25mohm, PD:2.5W  
Inductor: 3.3u20%13.5A(EPI0603H-3R3M-K01)(TTA), DCR=25mohm  
Output Cap: 1\*150U 6.3V(20%,ESR25,3528,H=1.9)

Ton	GND	VREF2 or Float	5V
Channel1 Fs	400 kHz	400 kHz	200 kHz
Channel2 Fs	500 kHz	300 kHz	300 kHz

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Title: 3.3V\_ALW/5V\_ALW (TPS51427A)  
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VDDQ and VTT discharge control

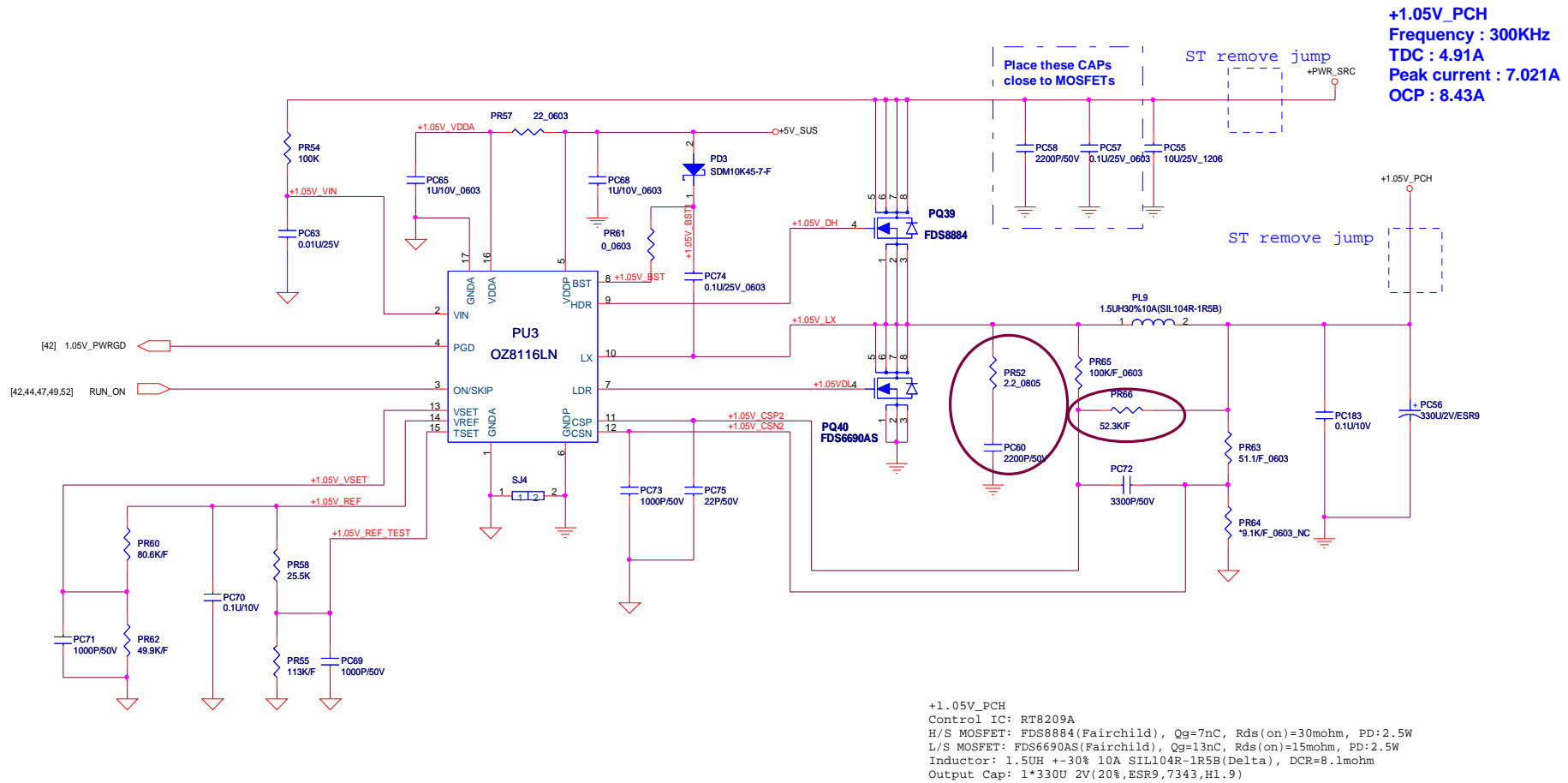
MODE pin	Discharge mode
V5IN	No discharge
VDDQ	Tracking discharge
S4/GND	Non-tracking discharge

VDDQ output voltage selection

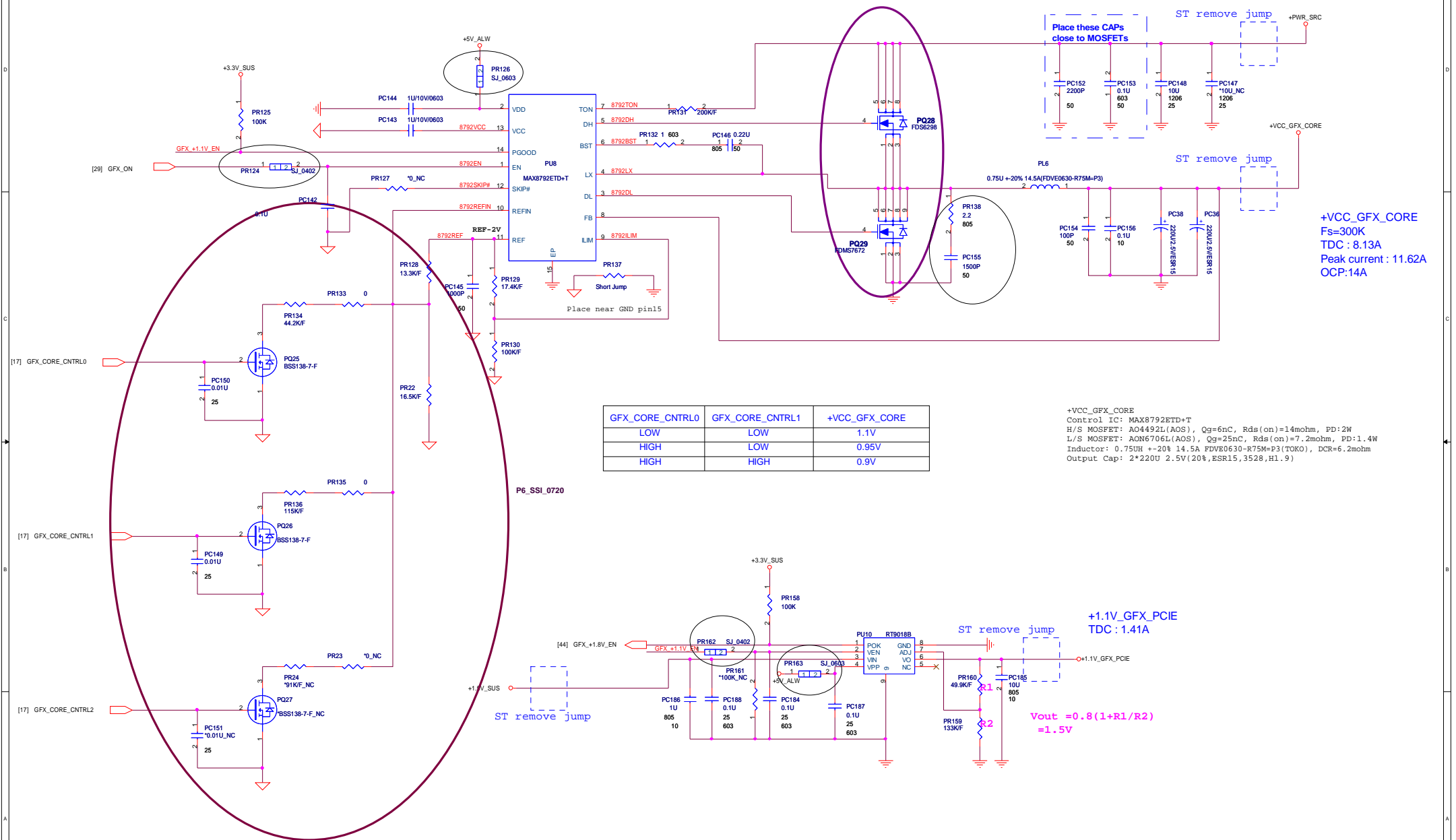
VDDQSET	VDDQ(V)	VTREF and VTT	NOTE
GND	1.5V	VDDQSNS/2	DDR3
V5IN	1.8V	VDDQSNS/2	DDR2
FB Resistors	Adjusting	VDDQSNS/2	1.5V < VVDDQ < 3V

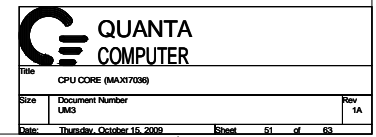
### Outputs Management by S3, S5 control

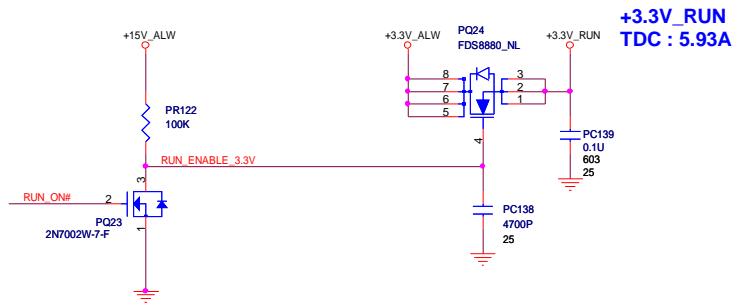
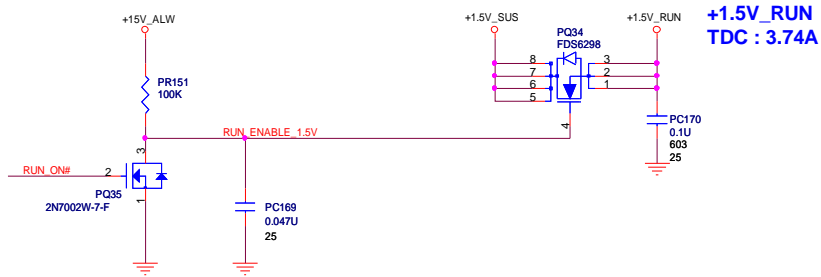
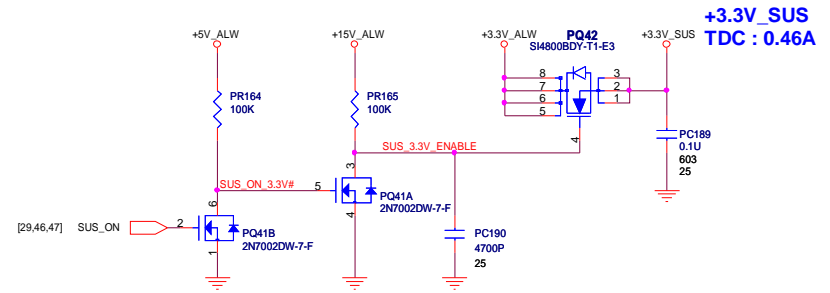
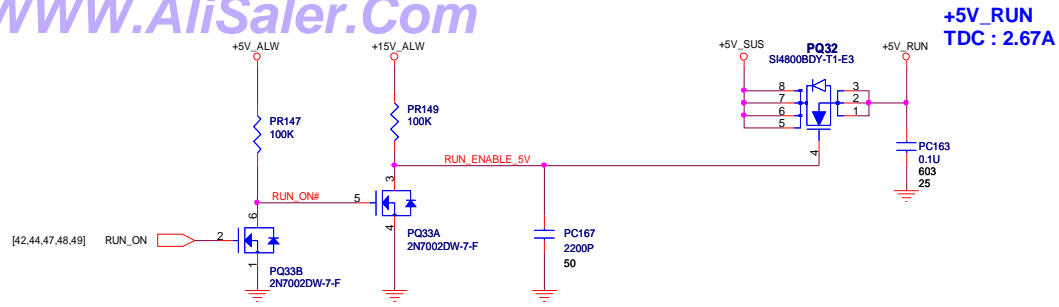
State	S3	S5	VDDQ	VTTREF	VTT
S0	HI	HI	On	On	On
S3	LO	HI	On	On	Off (Hi-Z)
S4/S5	LO	LO	On (discharge)	Off (discharge)	Off (discharge)





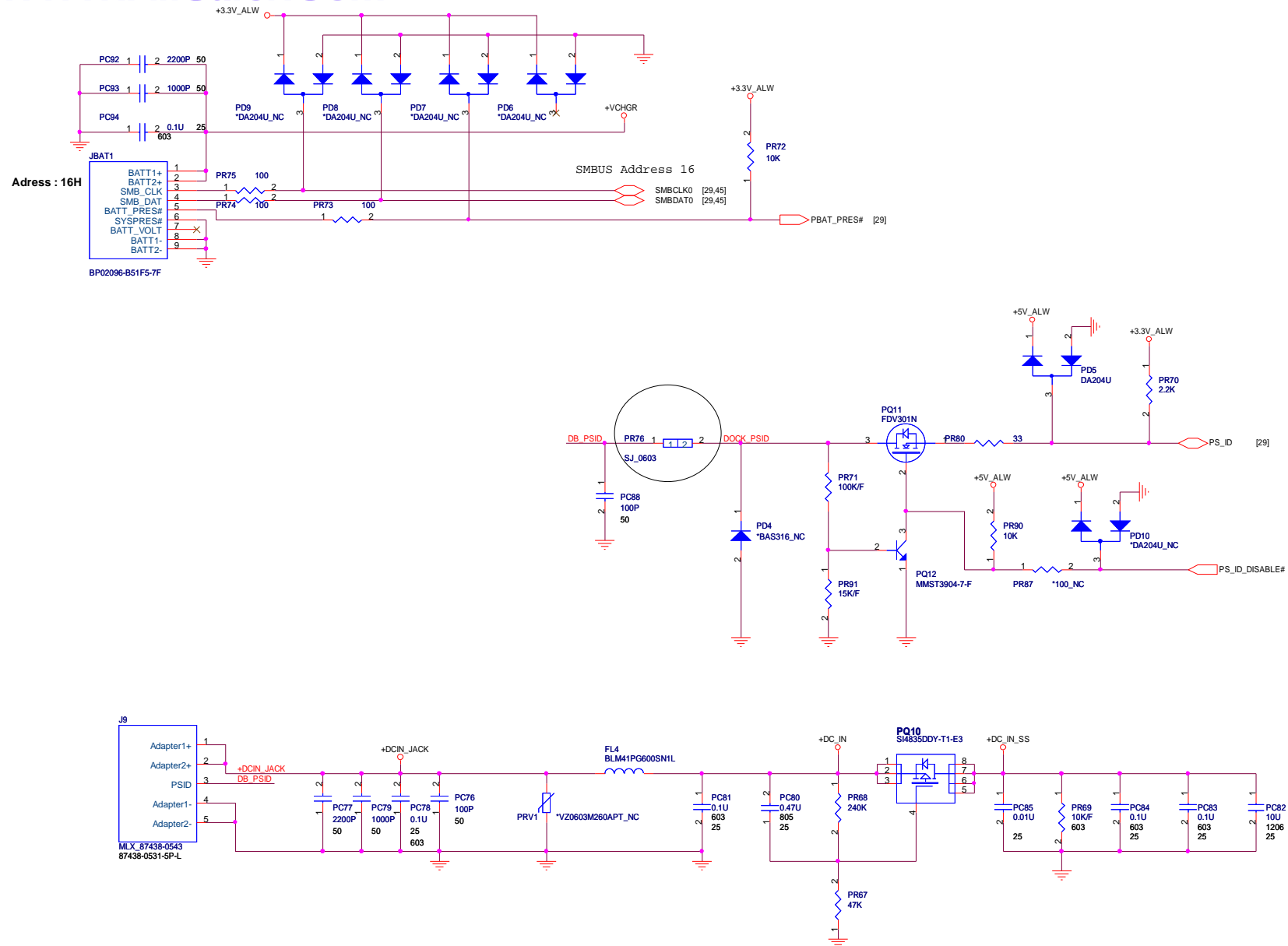


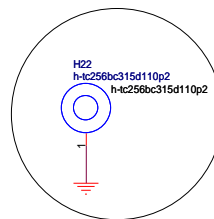
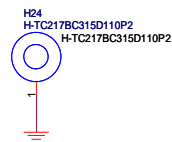
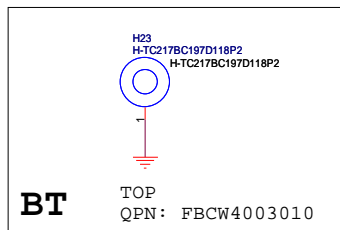
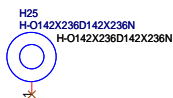
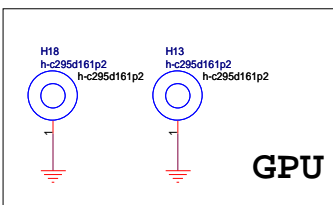
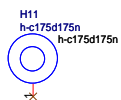
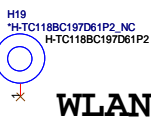
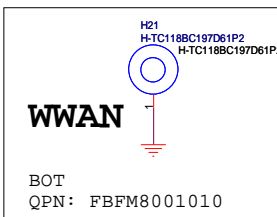
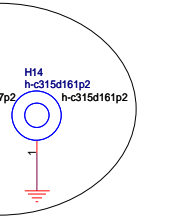
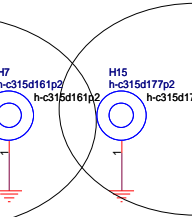
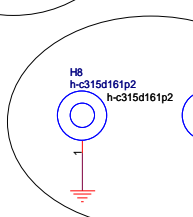
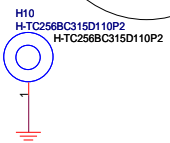
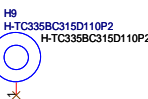
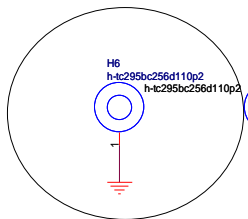
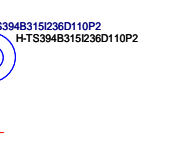
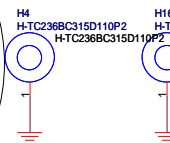
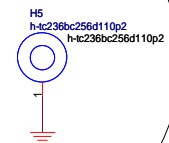
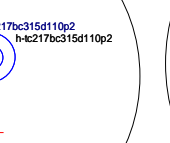
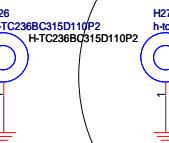
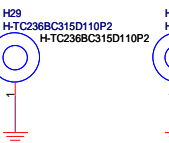
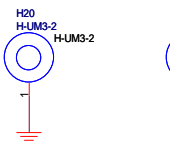
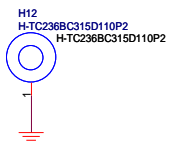
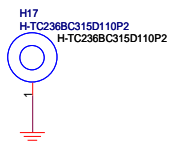
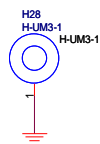
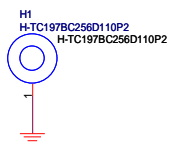





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